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Vishay/Siliconix
SI6410DQ-T1-E3

For any questions, you can email us directly:
sales@integrated-circuit.com

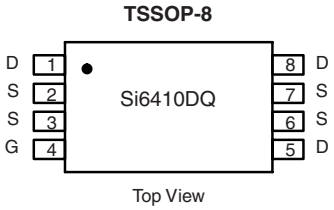
N-Channel 30-V (D-S) MOSFET

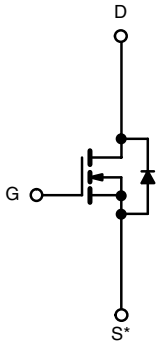
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.014 at V_{GS} = 10 V	± 7.8
	0.021 at V_{GS} = 4.5 V	± 6.3

FEATURES

- **Halogen-free**
- TrenchFET® Power MOSFETs

Pb-free
RoHS COMPLIANT





* Source Pins 2, 3, 6 and 7 must be tied common.

Ordering Information: Si6410DQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	± 7.8	A
	T_A = 70 °C		± 6.2	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.5	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	1.5	W
	T_A = 70 °C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Limit**	**Unit**
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes:
a. Surface Mounted on FR4 board, t ≤ 10 s.

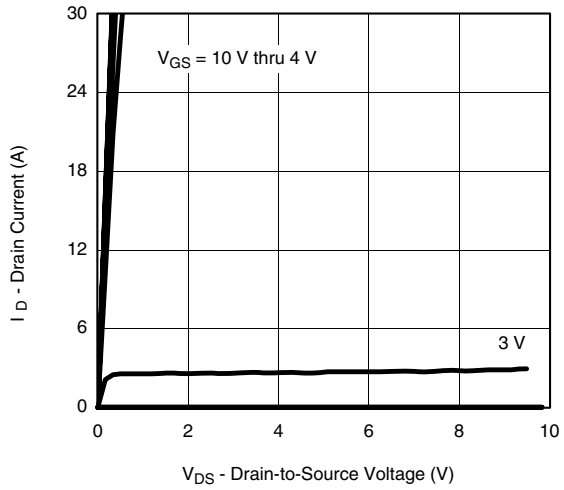
For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C			25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7.8 A		0.011	0.014	Ω
		V_{GS} = 4.5 V, I_D = 5 A		0.015	0.021	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 7.8 A		27		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.5 A, V_{GS} = 0 V		0.7	1.1	V
Dynamic[b]						
Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 5 V, I_D = 7.8 A		22	33	nC
Total Gate Charge	Q_{gt}	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 7.8 A		43	60	
Gate-Source Charge	Q_{gs}			9.0		
Gate-Drain Charge	Q_{gd}			7.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		15	30	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			70	120	
Fall Time	t_f			20	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.5 A, di/dt = 100 A/µs		50	80	

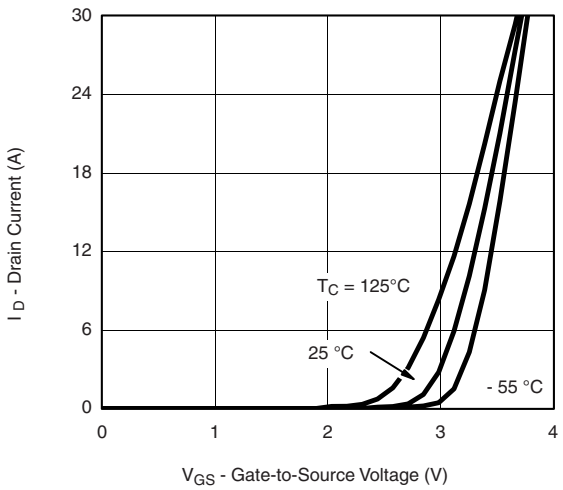
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

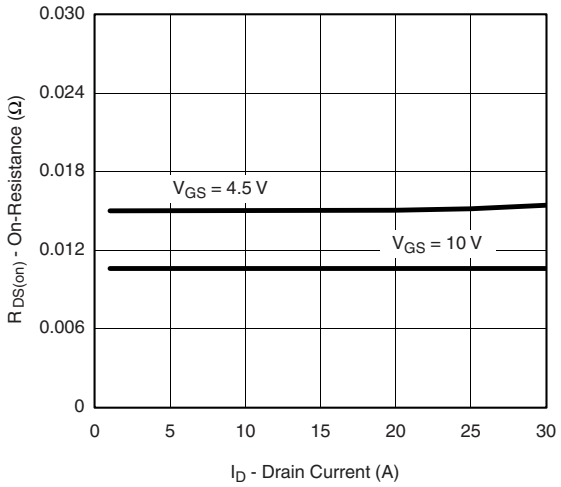
TYPICAL CHARACTERISTICS 25 °C unless noted



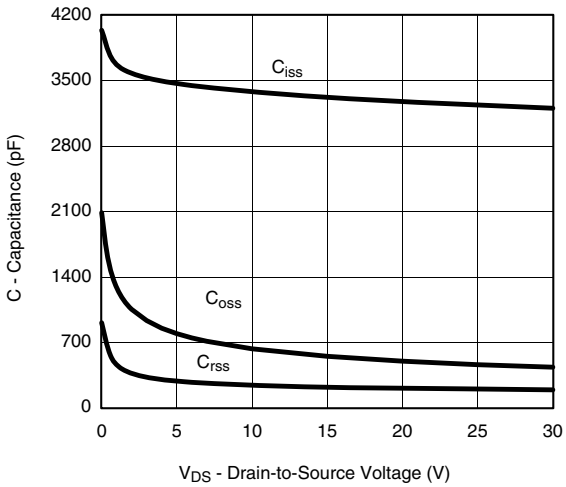
Output Characteristics



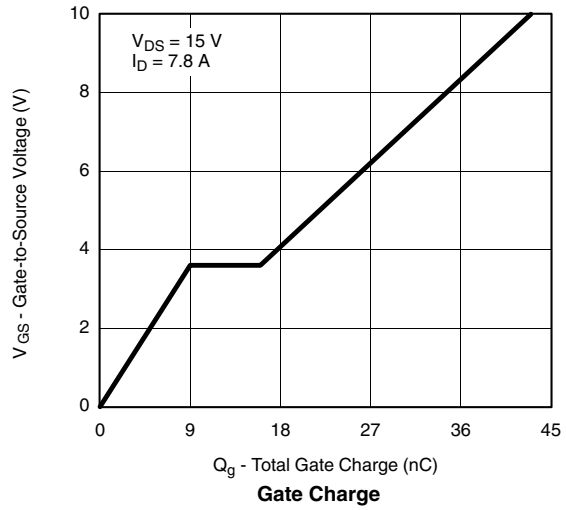
Transfer Characteristics



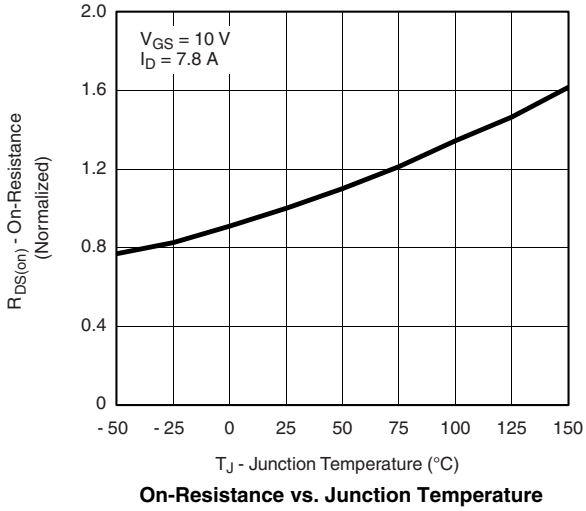
On-Resistance vs. Drain Current



Capacitance

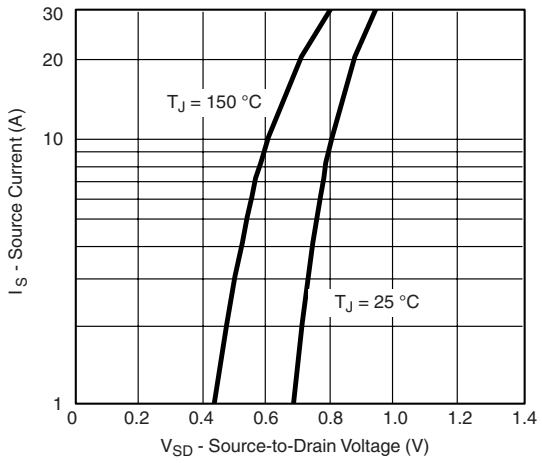


Gate Charge

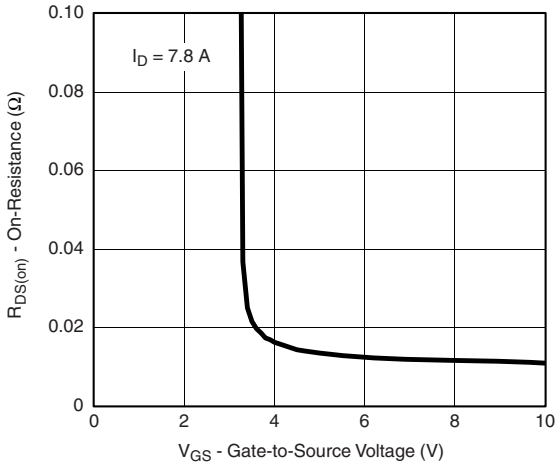


On-Resistance vs. Junction Temperature

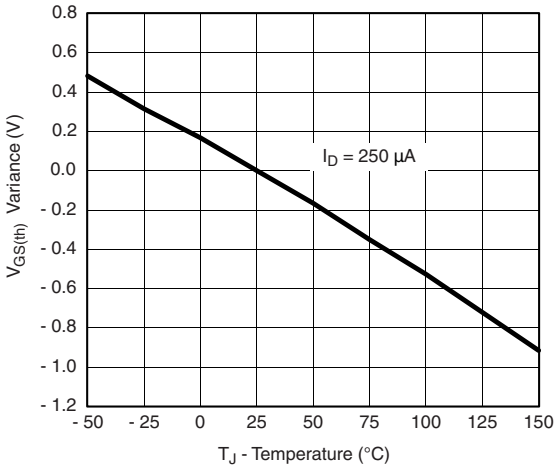
TYPICAL CHARACTERISTICS 25 °C unless noted



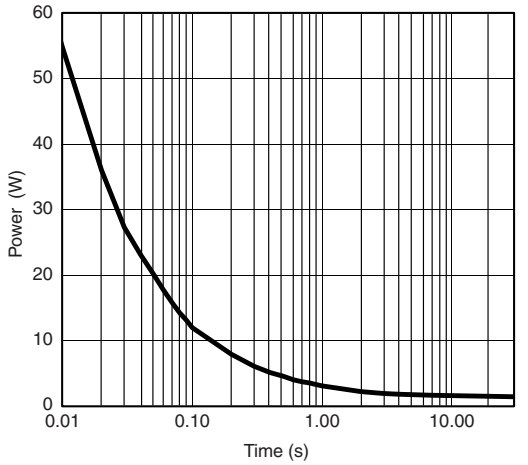
Source-Drain Diode Forward Voltage



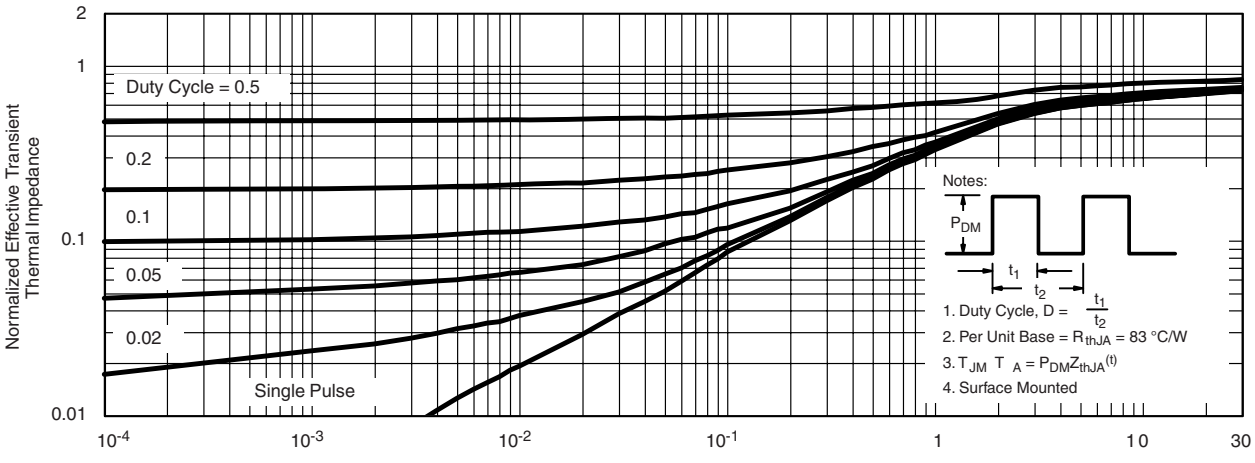
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

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