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ON Semiconductor MC100H643FNR2

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Distributor of ON Semiconductor: Excellent Integrated System Limited Datasheet of MC100H643FNR2 - IC CLK BUFFER 1:8 80MHZ 28PLCC Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

MC10H643, MC100H643

Dual Supply ECL to TTL 1:8 Clock Driver

Description

The MC10H/100H643 is a dual supply, low skew translating 1:8 clock driver. Devices in the ON Semiconductor H643 translator series utilize the PLCC-28 for optimal power pinning, signal flow through and electrical performance. The dual-supply H643 is similar to the H641, which is a single-supply 1:9 version of the same function.

The device features a 48 mA TTL output stage, with AC performance specified into a 50 pF load capacitance. A Latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldowns) the latch is transparent. A HIGH on the enable pin (\overline{EN}) forces all outputs LOW.

The 10H version is compatible with MECL 10H[™] ECL logic levels. The 100H version is compatible with 100K levels.

Features

- ECL/TTL Version of Popular ECLinPS[™] E111
- Low Skew Within Device 0.5 ns
- Guaranteed Skew Spec Part-to-Part 1.0 ns
- Latch
- Differential Internal Design
- V_{BB} Output
- · Dual Supply
- Reset/Enable
- Multiple TTL and ECL Power/Ground Pins
- Pb-Free Packages are Available*



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PLCC-28 FN SUFFIX CASE 776

MARKING DIAGRAM*



*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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Table 1. PIN DESCRIPTION

PIN	FUNCTION
OGND OVT IGND IVT V _{EE} V _{CCE} D, D V _{BB}	TTL Output Ground (0V) TTL Output V _{CC} (+5.0V) Internal TTL GND (0V) Internal TTL V _{CC} (+5.0V) ECL V _{EE} (-5.2/-4.5V) ECL Ground (0V) Signal Input (ECL) V _{BB} Reference Output
\overline{O} = \overline{O}	Enable Input (ECL)
LEN	Latch Enable Input (ECL)

Figure 1. Pinout: PLCC-28 (Top View)



Figure 2. Logic Diagram

Table 2. TRUTH TABLE

D	LEN	EN	Q
L	LLHX	L	L
H		L	H
X		L	Q _O
X		H	L



 Table 3. DC CHARACTERISTICS (IVT = OVT = $5.0 V \pm 5\%$; $V_{EE} = -5.2 V \pm 5\%$ (10H Version);

 $V_{EE} = -4.2 V \text{ to } -5.5 V$ (100H Version))

				0 °	C	25	°C	85	°C	
Symbol	Characteristic	:	Condition	Min	Мах	Min	Max	Min	Мах	Unit
I _{EE}		ECL	V _{EE} Pins	-	42	-	42	I	42	mA
I _{CCL}	Power Supply Current	TTL	Total all OVT	-	106	-	106	I	106	mA
I _{CCH}			and IVT pins	-	95	-	95	-	95	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 4. 10H ECL DC CHARACTERISTICS (IVT = OVT = 5.0 V ±[5%; V_{EE} = -5.2 V ±[5% (10H Version))

		0°	°C	25	°C	85	°C	
Symbol	Characteristic	Min	Max	Min	Max	Min	Мах	Unit
I _{INH} I _{INL}	Input HIGH Current Input LOW Current	_ 0.5	255 -	_ 0.5	175 -	_ 0.5	175 -	μA
V _{IH} V _{IL}	Input HIGH Voltage Input LOW Voltage	-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1070 -1950	-735 -1450	mV
V _{BB}	Output Reference Voltage	-1380	-1270	-1350	-1250	-1310	-1190	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 100H ECL DC CHARACTERISTICS (IVT = OVT = $5.0 \text{ V} \pm 5\%$; V_{EE} = -4.2 V to -5.5 V (100H))

		0	°C	25	°C	85	°C	
Symbol	Characteristic	Min	Мах	Min	Max	Min	Мах	Unit
I _{INH} I _{INL}	Input HIGH Current Input LOW Current	_ 0.5	255 -	_ 0.5	175 -	_ 0.5	175 -	μA
V _{IH} V _{IL}	Input HIGH Voltage Input LOW Voltage	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV
V _{BB}	Output Reference Voltage	-1380	-1260	-1380	-1260	-1380	-1260	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. DC TTL CHARACTERISTICS (IVT = OVT = 5.0 V ±[5%; V_{EE} = -5.2 V ±[5% (10H Version); V_{FF} = -4.2 V to -5.5 V (100H Version))

			0 °	C	25	°C	85	°C	
Symbol	Characteristic	Condition	Min	Мах	Min	Мах	Min	Мах	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = −3.0 mA I _{OH} = −15 mA	2.5 2.0	-	2.5 2.0	-	2.5 2.0	-	v
V _{OL}	Output LOW Voltage	I _{OH} = 48 mA	-	0.5	-	0.5	-	0.5	V
IOS	Output Short Circuit Current	V _{OUT} = 0 V	-100	-225	-100	-225	-100	-225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.



			0 °	С	25	°C	85	°C	
Symbol	Characteristic	Condition	Min	Мах	Min	Max	Min	Мах	Unit
t _{PLH}	Propagation Delay to Output D LEN EN	CL = 50 pF	4.0 3.5 3.5	5.0 5.5 5.5	4.1 3.5 3.5	5.1 5.5 5.5	4.4 3.9 3.9	5.4 5.9 5.9	ns
t _{skew}	Within-Device Skew	(Note 1)	_ !	0.5	-	0.5		0.5	ns
tw	Pulse Width Out HIGH or LOW @ f _{out} = 50MHz	CL = 50 pF (Note 2)	9.0	11.0	9.0	11.0	9.0	11.0	ns
t _s	Setup Time D		0.75	_	0.75	-	0.75	-	ns
t _h	Hold Time D		0.75	_	0.75	_	0.75	_	ns
t _{RR}	Recovery Time LEN EN		1.25 1.25		1.25 1.25		1.25 1.25	-	ns
t _{pw}	Minimum Pulse Width LEN EN		1.5 1.5	_	1.5 1.5	-	1.5 1.5		ns
t _r t _f	Rise / Fall Times 0.8 V – 2.0 V	CL = 50 pF	_	1.2	-	1.2	-	1.2	ns

Table 7. AC CHARACTERISTICS (IVT = OVT = 5.0 V ±∏5%; V_{EE} = -5.2 V ±∏10% (10H); -4.2 V to -5.5 V (100H); V_{CCE} = GND)

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Within-Device skew defined as identical transitions on similar paths through a device.

2. Pulse width is defined relative to 1.5 V measurement points on the output waveform.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10H643FN	PLCC-28	37 Units / Rail
MC10H643FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC10H643FNR2	PLCC-28	500 / Tape & Reel
MC10H643FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel
MC100H643FN	PLCC-28	37 Units / Rail
MC100H643FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC100H643FNR2	PLCC-28	500 / Tape & Reel
MC100H643FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Resource F	Ref	erence of Application Notes
AN1405/D	-	ECL Clock Distribution Techniques
AN1406/D	-	Designing with PECL (ECL at +5.0 V)
AN1503/D	-	ECLinPS [™] I/O SPiCE Modeling Kit
AN1504/D	-	Metastability and the ECLinPS Family
AN1568/D	-	Interfacing Between LVDS and ECL
AN1672/D	-	The ECL Translator Guide
AND8001/D	-	Odd Number Counters Design
AND8002/D	-	Marking and Date Codes
AND8020/D	-	Termination of ECL Logic Devices
AND8066/D	-	Interfacing with ECLinPS
AND8090/D	_	AC Characteristics of ECL Devices



PACKAGE DIMENSIONS





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