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AD7572AJN10

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Datasheet of AD7572AJN10 - IC ADC 12BIT LC2MOS HS 24-DIP

ANALOG DEVICES

LC²MOS Complete, High Speed 12-Bit ADC

AD7572A

FEATURES

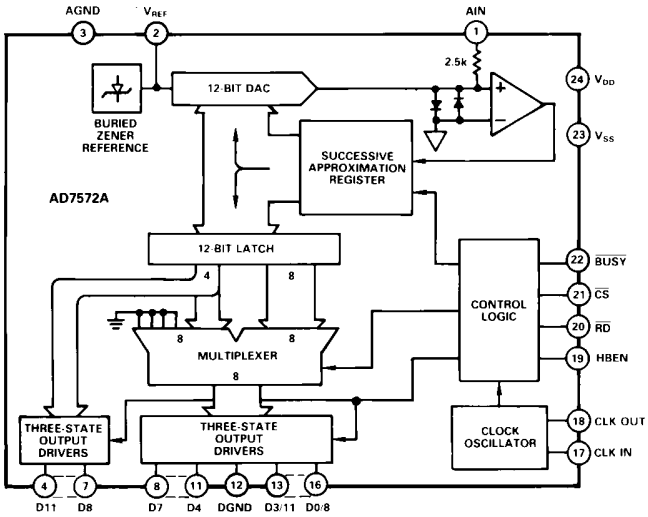
Improved AD7572
- **Faster Conversion Time**
  - **AD7572AXX03: 3 μs**
  - **AD7572AXX10: 10 μs**
- **5 V and −12 V or −15 V Power Supply Operation**
- **Better Offset and Gain Error Specifications**

Extended Plastic Temperature Range (−40°C to +85°C)

Low Power: 100 mW

Small 24-Pin, 0.3″ Wide DIP and SOIC DIP Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7572A is an enhanced replacement for the industry standard AD7572. Improvements include faster conversion times of 3 μs for the AD7572AXX03 and 10 μs for the AD7572AXX10. The required power supplies are 5 V and −12 V or −15 V. Additional features are better offset and gain error specifications over the original AD7572.

The AD7572A is a complete 12-bit ADC that offers high speed performance combined with low, CMOS power levels. The part uses an accurate, high speed DAC and comparator in a successive-approximation loop to achieve a fast conversion time. An on-chip buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range and the specified accuracy is achieved without any user trims. An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation, or the clock input may be driven from an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572A are decoupling capacitors for the supply voltages and reference output.

The AD7572A has a high speed digital interface with three-state data outputs and can operate under the control of standard microprocessor Read ($\overline{RD}$) and decoded address ($\overline{CS}$) signals. Interface timing is sufficiently fast to allow the AD7572A to operate with most microprocessors, with three-state enable times of only 90 ns and bus relinquish times of 75 ns.

The AD7572A is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while retaining low CMOS power levels.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   Fast, 3 μs and 10 μs conversion times make the AD7572A ideal for DSP applications and wideband data acquisition systems.
2. Wide Power Supply Range
   The AD7572A operates from 5 V and −12 V or −15 V power supplies.
3. Microprocessor Interface
   Fast, easy-to-use digital interface has three-state bus access times of 90 ns and bus relinquish times of 75 ns allowing the AD7572A to interface to most microprocessors.
4. Low Power
   LC²MOS circuitry gives low power drain (100 mW) from +5, −12 volt supplies.
5. 24-pin 0.3″ DIP and SOIC packages offer space saving over parts in 28-pin 0.6″ DIP.

REV. A

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AD7572A—SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{SS} = −11.4 V to −16.5 V, AGND = DGND = 0 V, f_{CLK}: 4.0 MHz for AD7572AXX03, 1.25 MHz for AD7572AXX10. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode.)

Parameter	J, A Versions[1]	L Version[1]	S Version[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity @ 25°C	±1	±1/2	±1	LSB max	
T_{min} to T_{max}	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Offset Error @ 25°C	±2	±2	±2	LSB max	
T_{min} to T_{max}	±4	±4	±4	LSB max	Typical Change over Temp is ±1 LSB
Full Scale (FS) Error[2] @ 25°C	±8	±8	±8	LSB max	FS = 5 V
Full Scale TC[3, 4]	45	25	45	ppm/°C max	Ideal Last Code Transition = FS −3/2 LSBs
ANALOG INPUT					
Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	For Bipolar Operation See Figures 10
Input Current	3.5	3.5	3.5	mA max	and 12
INTERNAL REFERENCE VOLTAGE					
V_{REF} Output @ 25°C	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	V min/V max	−5.25 V ±1%
V_{REF} Output TC	40	20	40	ppm/°C typ	External Load Should Not
Output Current Sink Capability	550	550	550	µA max	Change During Conversion
POWER SUPPLY REJECTION					
V_{DD} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{SS} = −12 V or −15 V V_{DD} = 4.5 V to 5.5 V
V_{SS} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{DD} = 5 V V_{SS} = −11.4 V to −16.5 V
LOGIC INPUTS					
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN					
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{DD} = 5 V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	V min	
C_{IN}, Input Capacitance[5]	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, HBEN					
I_{IN}, Input Current	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
CLK IN					
I_{IN}, Input Current	±20	±20	±20	µA max	V_{IN} = 0 V to V_{DD}
LOGIC OUTPUTS					
D11–D0/8, $\overline{BUSY}$, CLK OUT					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200 µA
D11–D0/8					
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
AD7572AXX03					
Synchronous Clock	3.125	3.125	3.125	µs max	f_{CLK} = 4 MHz. See Under
Asynchronous Clock	3/3.25	3/3.25	3/3.25	µs min/µs max	Control Inputs Synchronization
AD7572AXX10					
Synchronous Clock	10	10	–	µs max	f_{CLK} = 1.25 MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	–	µs min/µs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−12 to −15	−12 to −15	−12 to −15	V nom	−11.4 V to −16.5 V for Specified Performance
I_{DD}[6]	7	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5 V
I_{SS}[6]	10	10	12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5 V
Power Dissipation	100	100	120	mW typ	V_{SS} = −12 V
	155/185	155/185	179/215	mW max	V_{SS} = −12 V/−15 V

NOTES
[1]Temperature ranges are as follows: J, L Versions, 0 to +70°C; A Version, −40°C to +85°C; S Version, −55°C to +125°C.
[2]Includes internal voltage reference error.
[3]Full-Scale TC = ΔFS/ΔT where ΔFS is Full-Scale change from T_A = +25°C to T_{min} or T_{max}.
[4]Includes internal voltage reference drift.
[5]Sample tested to ensure compliance.
[6]Power supply current is measured when the AD7572A is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.
Specifications subject to change without notice.

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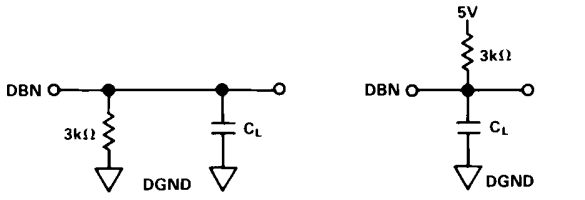
TIMING CHARACTERISTICS[1] (V_{DD} = 5 V ± 5%, V_{SS} = −11.4 V to −16.5 V)

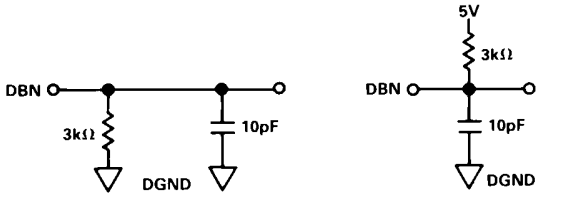
Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, L, A Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L=20 pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L=100 pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	15	15	15	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	0	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	200	200	200	ns min	Delay Between Successive Read Operations

NOTE
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6) *b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to −17 V
AGND to DGND . . . . . −0.3 V, V_{DD} + 0.3 V
AIN to AGND . . . . . −15 V to +15 V
Digital Input Voltage to DGND
(CLK IN, HBEN, $\overline{RD}$, $\overline{CS}$) . . . . . −0.3 V, V_{DD} +0.3 V
Digital Output Voltage to DGND
(D11-D0/8, CLK OUT, $\overline{BUSY}$) . . . . . −0.3 V, V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, L Versions) . . . . . 0 to +70°C
Industrial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1,000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

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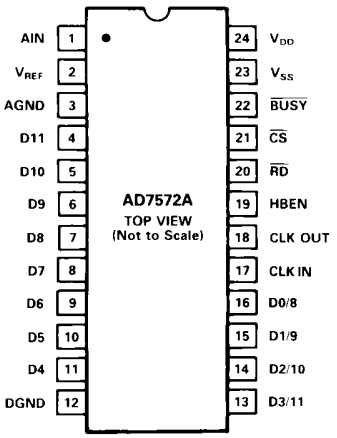
ORDERING GUIDE

Model	Conversion Time	Temperature Range	Full-Scale TC	Accuracy Grade	Package Option[1]
AD7572AJN03	3 μs	0°C to +70°C	45 ppm/°C	±1 LSB	N-24
AD7572AAN03	3 μs	−40°C to +85°C	45 ppm/°C	±1 LSB	N-24
AD7572ASQ03[2]	3 μs	−55°C to +125°C	45 ppm/°C	±1 LSB	Q-24
AD7572ALN03	3 μs	0°C to +70°C	25ppm/°C	±1/2 LSB	N-24
AD7572AAQ03	3 μs	−40°C to +85°C	45 ppm/°C	±1 LSB	Q-24
AD7572AJR03	3 μs	0°C to +70°C	45 ppm/°C	±1 LSB	R-24
AD7572AAR03	3 μs	−40°C to +85°C	45 ppm/°C	±1 LSB	R-24
AD7572AJN10	10 μs	0°C to +70°C	45 ppm/°C	±1 LSB	N-24
AD7572AAN10	10 μs	−40°C to +85°C	45 ppm/°C	±1 LSB	N-24
AD7572ALN10	10 μs	0°C to +70°C	25 ppm/°C	±1/2 LSB	N-24
AD7572AJR10	10 μs	0°C to +70°C	45 ppm/°C	±1 LSB	R-24

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC).
[2]AD7572ASQ03 will be available to /883B processing only. Contact your local sales office for release information.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	AIN	Analog Input.
2	V_{REF}	Voltage Reference Output. The AD7572A has its own internal −5.25 V reference.
3	AGND	Analog Ground.
4 . . . 11	D11 . . . D4	Three State Data Outputs. They become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
13 . . . 16	D3/11 . . . D0/8	Individual pin function is dependent upon High Byte Enable (HBEN) Input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

NOTES
*D11 . . . D0/8 are the ADC data output pins.
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB.

12	DGND	Digital Ground.
17	CLK IN	Clock Input Pin. An external TTL compatible clock may be applied to this pin. Alternatively, a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description for crystal (resonator).
19	HBEN	High Byte Enable Input. Its primary function is to multiplex the 12 bits of conversion data onto the lower D7 . . . D0/8 outputs (4 MSBs or 8 LSBs). See Pin Description 4 . . . 11 and 13 . . . 16. It also disables conversion start when HBEN is high.
20	$\overline{RD}$	READ Input. This active LOW signal, in conjunction with $\overline{CS}$, is used to enable the output data three-state drivers and initiate a conversion if $\overline{CS}$ and HBEN are low.
21	$\overline{CS}$	CHIP SELECT Input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiate a conversion if $\overline{RD}$ and HBEN are low.
22	$\overline{BUSY}$	$\overline{BUSY}$ Output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
23	V_{SS}	Negative Supply, −12 V to −15 V.
24	V_{DD}	Positive Supply, +5 V.

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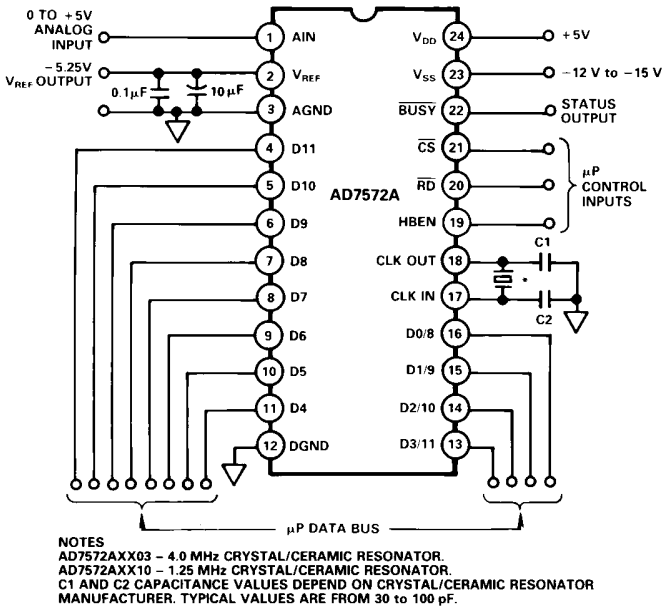
OPERATIONAL DIAGRAM

An operational diagram for the AD7572A is shown in Figure 3. The AD7572A is a 12-bit successive approximation A/D converter. The addition of just a crystal/ceramic resonator and a few capacitors enables the device to perform the analog-to-digital function.



NOTES
AD7572AXX03 – 4.0 MHz CRYSTAL/CERAMIC RESONATOR.
AD7572AXX10 – 1.25 MHz CRYSTAL/CERAMIC RESONATOR.
C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30 to 100 pF.

Figure 3. AD7572A Operational Diagram

CONVERTER DETAILS

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit voltage mode DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 4, the AIN input connects to the comparator input via 2.5 kΩ.

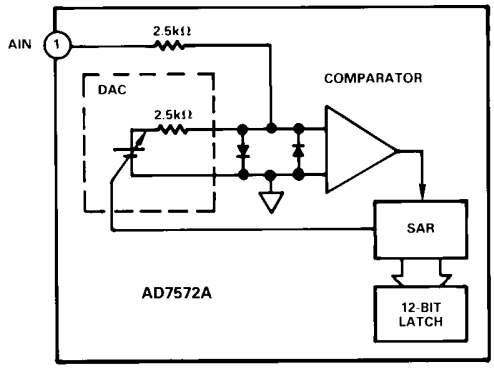


Figure 4. AD7572A AIN Input

The DAC which has a similar 2.5 kΩ output impedance connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output. The MSB decision is made 80 ns (typically) after the second falling edge of CLK IN following a conversion start. Similarly, the succeeding bit decisions are made approximately 80 ns after a CLK IN edge until conversion is finished. At the end of conversion, the DAC output current balances the AIN input current. The SAR contents (12-bit data word) which represent the AIN input signal is loaded into a 12-bit latch.

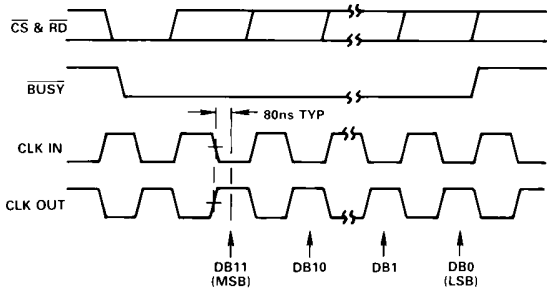


Figure 5. Operating Waveforms Using an External Clock Source for CLK IN

CONTROL INPUTS SYNCHRONIZATION

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach ensures a fixed 3.125 μs conversion time for the AD7572AXX03 and 10 μs for the AD7572AXX10: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT.

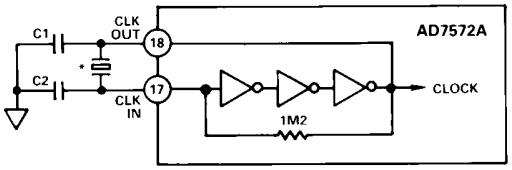
DRIVING THE ANALOG INPUT

During conversion, the AIN input current is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 4 MHz when CLK IN = 4 MHz). The analog input voltage must remain fixed during this period and as a result must be driven from an op amp or sample-and-hold with a low output impedance. The output impedance of an op amp is equal to the open loop output impedance divided by the loop gain at the frequency of interest.

Suitable devices capable of driving the AD7572A AIN input are the AD845 op amp or the AD585 sample-and-hold.

INTERNAL CLOCK OSCILLATOR

Figure 6 shows the AD7572A internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for the ADC timing. Alternatively the crystal/resonator may be omitted and an external clock source may be connected to CLK IN. For an external clock the mark/space ratio can vary from 45/55 to 55/45. An inverted CLK IN signal will appear at the CLK OUT pin as shown in the operating waveforms of Figure 5.



NOTES
AD7572AXX03 – 4.0 MHz CRYSTAL/CERAMIC RESONATOR.
AD7572AXX10 - 1.25 MHz CRYSTAL/CERAMIC RESONATOR.
C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30 to 100 pF.

Figure 6. AD7572A Internal Clock Circuit

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INTERNAL REFERENCE

The AD7572A has an on-chip, buffered, temperature-compensated, buried Zener reference, which is factory trimmed to −5.25 V ±1%. It is internally connected to the DAC and is also available at Pin 2 to provide up to 550 μA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter out wideband noise from the reference diode (10 μF of tantalum in parallel with 100 nF ceramic). Some applications will use the AD7572A as an upgrade replacement for the AD7572. The recommended reference decoupling for the AD7572 differs from the AD7572A in that it contains an additional 10 Ω resistor in series with the capacitors. This resistor makes no difference to the performance of the 10 μs version of the AD7572A, but it does adversely affect the linearity performance of the 3 μs version. So, applications using the AD7572A as a 3 μs upgrade of the AD7572 must replace the 10 Ω reference resistor with a wire link.

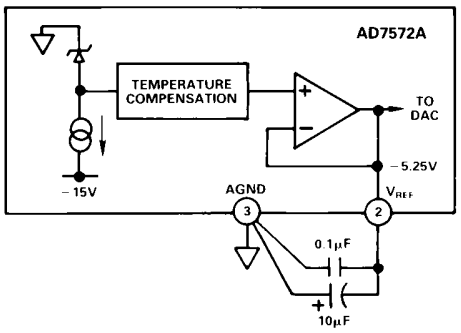

Figure 7. AD7572A Internal −5.25 V Reference

UNIPOLAR OPERATION

Figure 8 shows the ideal input/output characteristic for the 0 to 5 volt input range of the AD7572A. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS–3/2 LSBs). The output code is natural binary with 1 LSB = FS/4096 = (5/4096) V = 1.22 mV.

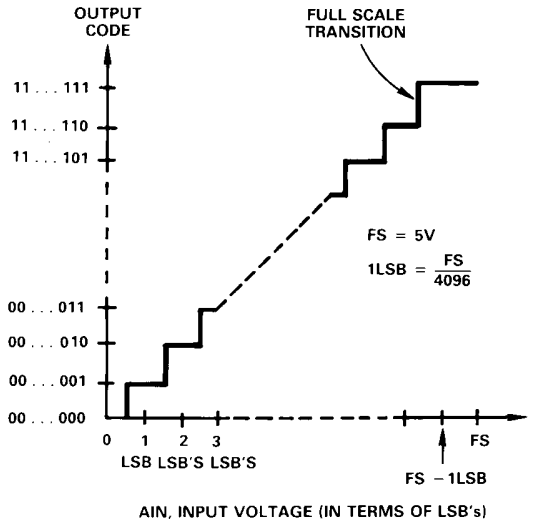

Figure 8. AD7572A Ideal Input/Output Transfer Characteristic

UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

In applications where absolute accuracy is important then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 9 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving AIN (i.e., A1 in Figure 9.). For zero offset error apply 0.61 mV (i.e., 1/2 LSB) at V_{IN} and adjust the op-amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

For zero full-scale error apply an analog input of 4.99817 V (i.e., FS–3/2 LSBs or last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

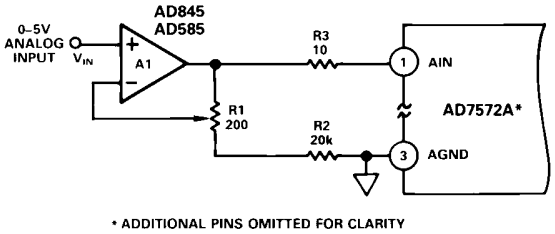

Figure 9. Unipolar 0 to +5 V Operation with Gain Error Adjust

BIPOLAR OPERATION

Figures 10 and 12 show how bipolar operation can be achieved with the AD7572A. Both circuits use an op amp to offset the analog signal (V_{IN}) by 2.5 V. Alternatively, the op amp (A1) can be replaced by a sample hold as shown in Figure 24. The op amp transfer functions are given below:

Figure 10: AIN = (V_{IN} + 2.5) volts
Figure 12: AIN = (−V_{IN} + 2.5) volts

Both circuits have an analog input range of ±2.5 V and an LSB size of 1.22 mV. The output codes are offset binary for Figure 10 and complementary offset binary for Figure 12. Their ideal input/output transfer characteristics after offset and full-scale adjustment are shown in Figures 11 and 13.

Signal ranges other than ±2.5 V are easily accommodated using different values of R3 and R4 for Figure 10, and a different R2 value for Figure 12. These resistors should be chosen such that the voltage range at AIN covers the full dynamic range (i.e., 0 V to 5 V) of the ADC. All resistors should be the same type and from the same manufacturer so that their temperature coefficients match.

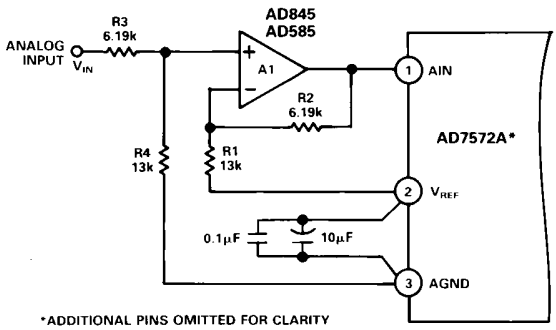

Figure 10. AD7572A Bipolar Operation – Output Code is Offset Binary

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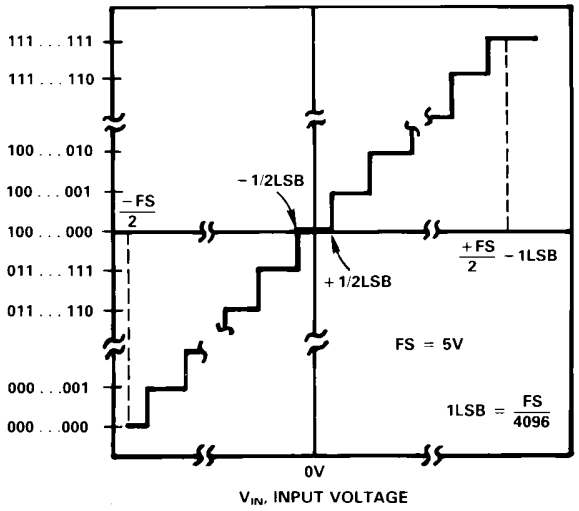

Figure 11. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 10

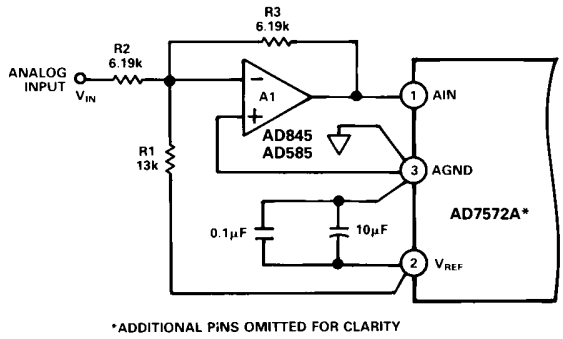

Figure 12. AD7572A Bipolar Operation - Output Code is Complementary Offset Binary

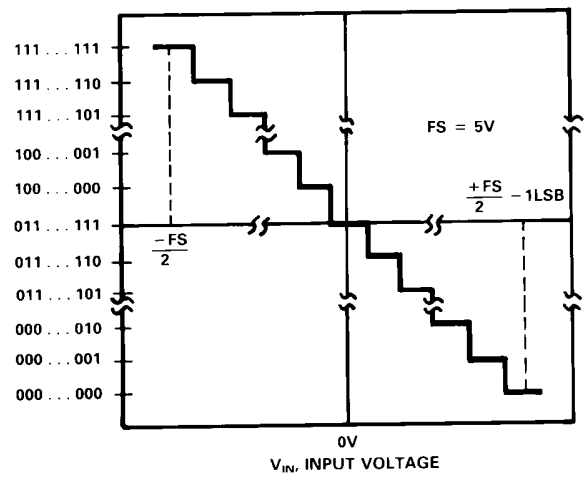

Figure 13. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 12

OFFSET AND FULL-SCALE ERROR

In most Digital Signal Processing (DSP) applications offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an analog signal is quantized, digitally processed and recreated using a DAC. In these types of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important parameter in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

In measurement applications where absolute accuracy is required, offset and full-scale error can be adjusted to zero as in Figure 14.

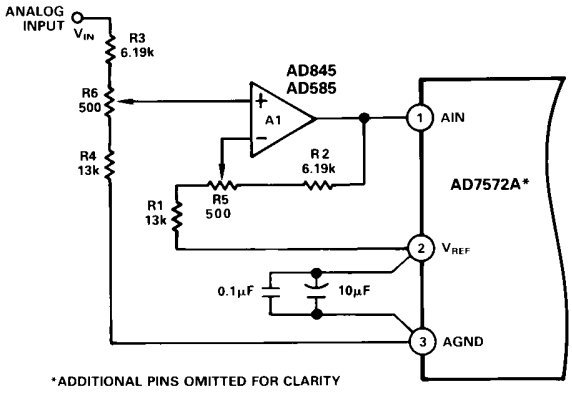

Figure 14. AD7572A Bipolar Operation with Offset and Gain Error Adjust

BIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

The bipolar circuit of Figure 10 can be adjusted for offset and full-scale errors, by including two potentiometers R5 and R6, as shown in Figure 14. Offset must be adjusted before full-scale error. This is achieved by applying an analog input of 0.61 mV (1/2 LSB) at V_{IN} and adjusting R5 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

For full-scale error adjustment, the analog input must be at 2.49817 volts (i.e., FS/2 –3/2 LSBs or last transition point). Then R6 is adjusted until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

A similar offset and full-scale error adjustment procedure may be employed for Figure 12 by making R1 and R2 variable. Offset must again be adjusted before full scale error. This is achieved by applying an analog input of 0.61 mV at V_{IN} and adjusting R1 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

For full-scale error adjustment, apply a signal source of 2.49817 V at V_{IN} and adjust R2 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

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APPLICATION HINTS

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the AD7572A a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the AD7572A. The analog input should be screened by AGND.

A single point analog ground (STAR ground) separate from the logic system ground should be established at Pin 3 (AGND) or as close as possible to the AD7572A as shown in Figure 15. Pin 12 (AD7572A DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between the signal source and the ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7572A data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the AD7572A data bus.

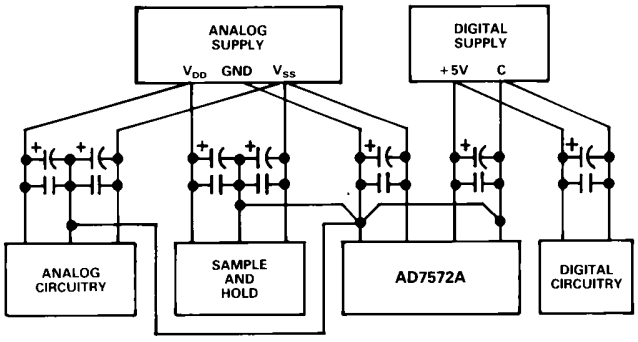

Figure 15. Power Supply Grounding Practice

TIMING AND CONTROL

Conversion start and data read operations are controlled by three AD7572A digital inputs; HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 16 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required on all three inputs to initiate a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

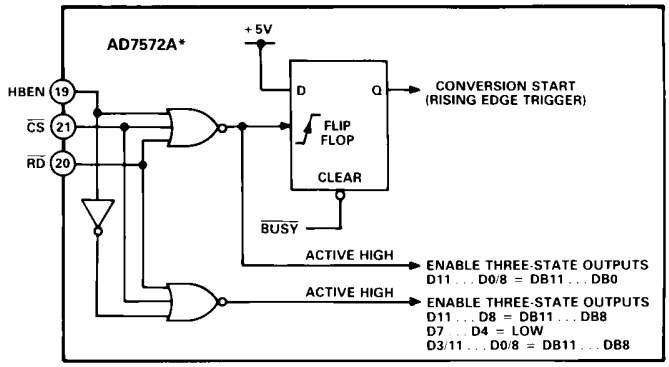

Figure 16. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

There are two modes of operation as outlined by the timing diagrams of Figures 17 to 20. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode which does not require microprocessor WAIT states, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

DATA FORMAT

The output data format can either be a complete parallel load (DB11 . . . DB0) for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7 . . . D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7 . . . D0/8 outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSBs always appear on D11 . . . D8 whenever the three-state output drivers are turned on.

SLOW MEMORY MODE, PARALLEL READ (HBEN = LOW)

Figure 17 and Table I show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the AD7572A acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11 . . . D0/8.

SLOW MEMORY MODE, TWO BYTE READ

For a two byte read only 8 data outputs D7 . . . D0/8 are used. Conversion start procedure and data output status for the first read operation is identical to Slow Memory Mode, Parallel Read. See Figure 18 timing diagram and Table II data bus status. At the end of conversion the low data byte (DB7 . . . DB0) is read from the ADC. A second READ operation, with HBEN high, places the high byte on data outputs D3/11 . . . D0/8 and disables conversion start. Note the 4MSBs appear on data outputs D11 . . . D8 during the two READ operations above.

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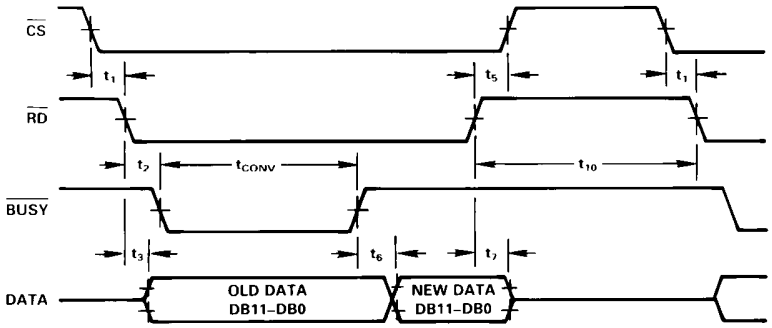

Figure 17. Slow Memory Mode, Parallel Read Timing Diagram

Table I. Slow Memory Mode, Parallel Read Data Bus Status

AD7572A Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

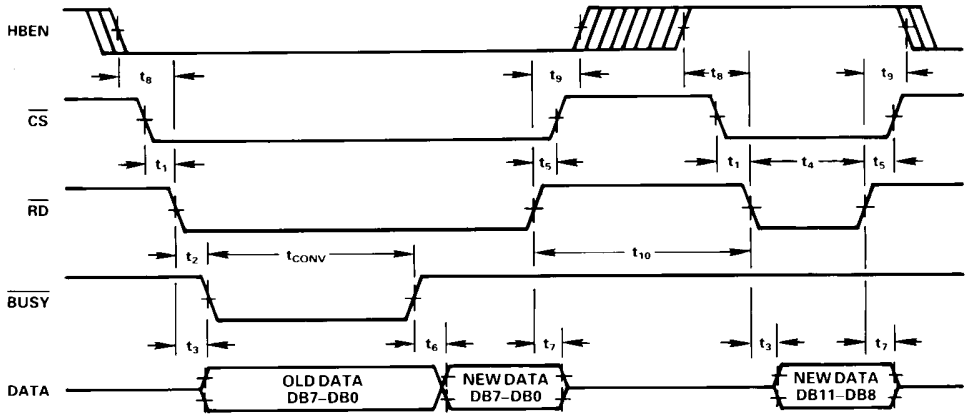

Figure 18. Slow Memory Mode, Two Byte Read Timing Diagram

Table II. Slow Memory Mode, Two Byte Read Data Bus Status

AD7572A Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

ROM MODE, PARALLEL READ (HBEN = LOW)

The ROM Mode avoids placing a microprocessor into a wait state. A conversion is started with a READ operation, and the 12-bits of data from the previous conversion are available on data outputs D11 . . . D0/8 (see Figure 19 and Table III). This data may be disregarded if not required. A second READ operation reads the new data (DB11 . . . DB0) and starts another conversion. A delay at least as long as the AD7572A conversion time must be allowed between READ operations.

ROM MODE, TWO BYTE READ

As previously mentioned for a two byte read, only data outputs D7 . . . D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM Mode, Parallel Read. See Figure 20 timing diagram and Table IV data bus status. Two more READ operations are required to access the new conversion result. A delay equal to the AD7572A conversion time must be allowed between conversion start and the second data READ operation. The second READ operation, with HBEN high, disables conversion start and places the high byte (4 MSBs) on data outputs D3/11 . . . D0/8. A third READ operation accesses the low data byte (DB7 . . . DB0) and starts another conversion. The 4MSBs appear on data outputs D11 . . . D8 during all three read operations above.

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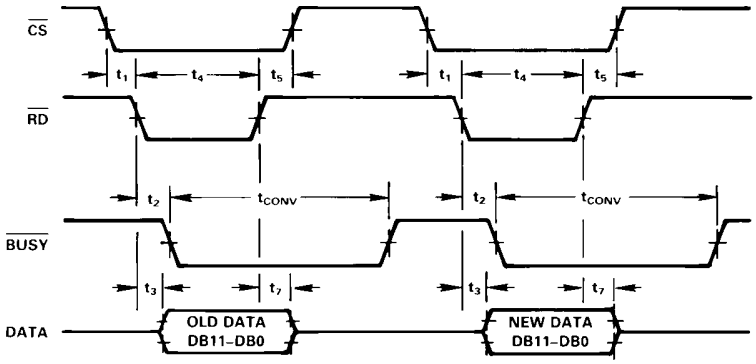

Figure 19. ROM Mode, Parallel Read Timing Diagram

Table III. ROM Mode, Parallel Read Data Bus Status

AD7572A Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

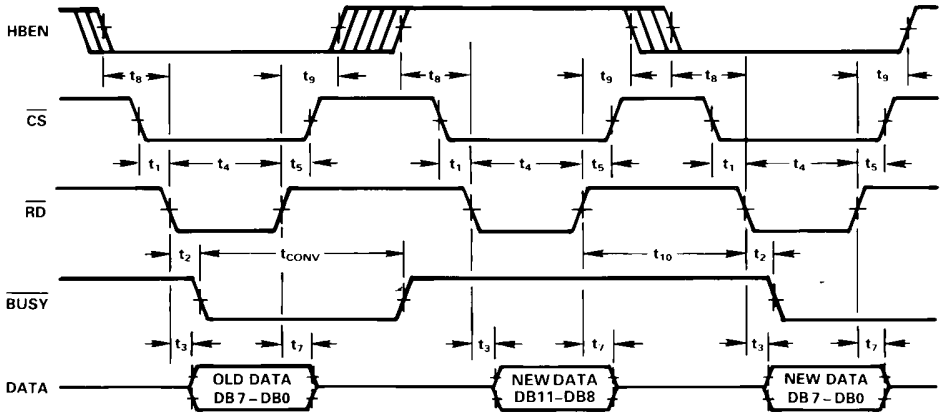

Figure 20. ROM Mode, Two Byte Read Timing Diagram

Table IV. ROM Mode, Two Byte Read Data Bus Status

AD7572A Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

MICROPROCESSOR INTERFACING

The AD7572A is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally connected to the microprocessor address bus.

MC68000 Microprocessor

Figure 21 shows a typical interface for the 68000. The AD7572A is operating in the Slow Memory Mode. Assuming the AD7572A is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result.

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$, so that the 68000 is forced into a WAIT state. At the end of conversion $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the μP.

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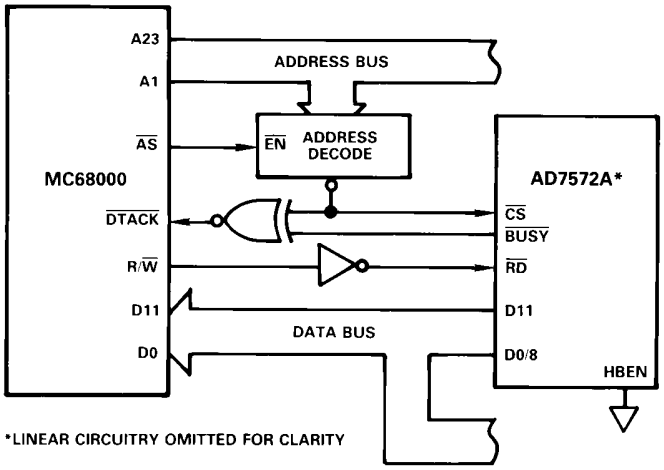

Figure 21. AD7572A–MC68000 Interface

8085A, Z80 MICROPROCESSOR

Figure 22 shows an AD7572A interface for the Z80 and 8085A. The AD7572A is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN, so that an even address (HBEN = LOW) to the AD7572A will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A LHLD (B000)
For the Z80 LD HL, (B000)

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{BUSY}$ forces the microprocessor to WAIT for the AD7572A conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

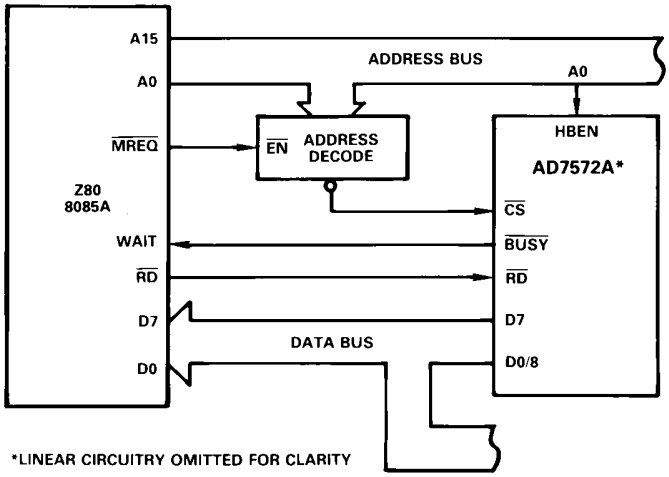

Figure 22. AD7572A–8085/Z80 Interface

TMS32010 MICROCOMPUTER

Figure 23 shows an AD7572A-TMS32010 interface. The AD7572A is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18 MHz but will typically work over the full TMS32010 clock frequency range.

The AD7572A is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into data memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

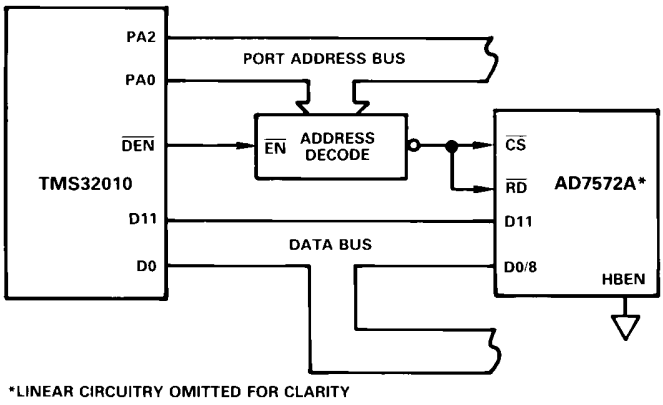

Figure 23. AD7572A–TMS32010 Interface

AD7572A–AD585 SAMPLE-HOLD INTERFACE

Figure 24 shows an AD585 sample-hold amplifier driving the AIN input of the AD7572A. The interface contains resistors R1, R2, R3 and R4 to allow a bipolar input signal range of ±2.5 volts. The maximum sampling frequency is 166 kHz for the AD7572AXX03 (3 μs conversion) and 77 kHz for the AD7572AXX10 (10 μs conversion). This includes the sample-hold amplifier acquisition time (3 μs).

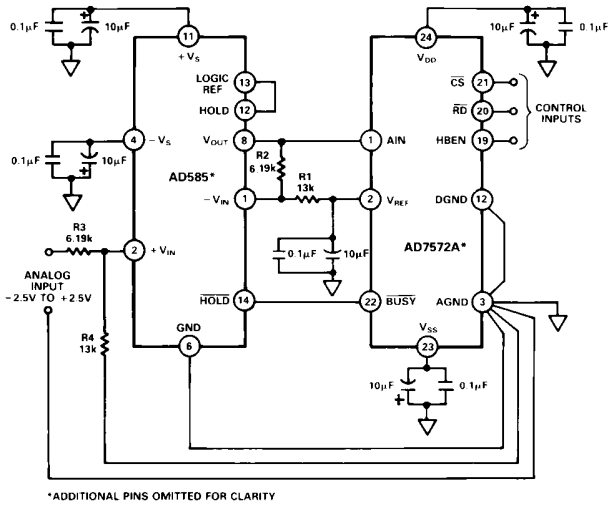

Figure 24. AD7572A–AD585 Sample-and-Hold Interface

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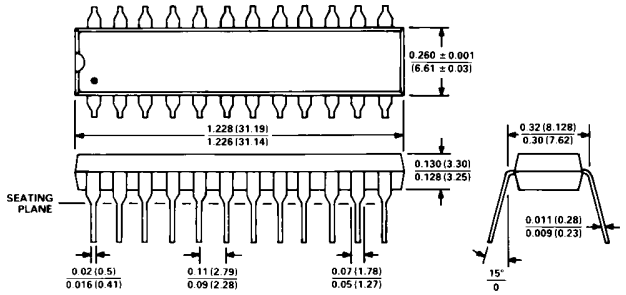
When an AD7572A conversion is initiated, the converter $\overline{BUSY}$ output goes low indicating conversion is in progress. The falling edge of this $\overline{BUSY}$ output signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7572A. When conversion is finished, the $\overline{BUSY}$ output returns HIGH allowing the sample-hold to track the input signal. To achieve the maximum sampling rate, the AD7572A output data must be read within 3 μs immediately after conversion while the sample-hold amplifier is acquiring the next sample.

OUTLINE DIMENSIONS

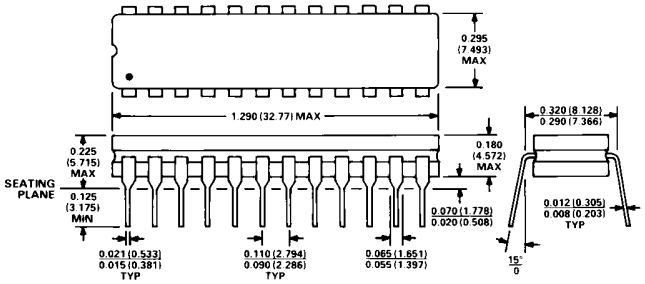
Dimensions shown in inches and (mm).

24-Pin Plastic DIP (N-24)



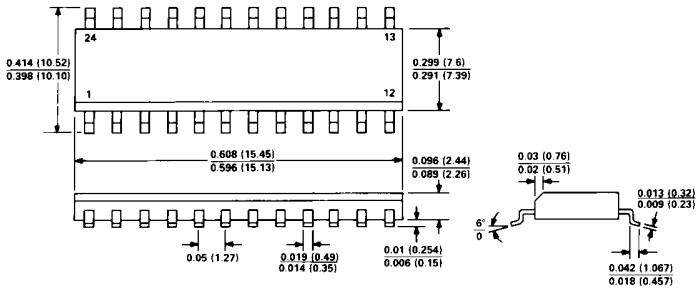
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN/LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Cerdip (Q-24)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Plastic SOIC (R-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

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