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STMicroelectronics
STGIPS20C60-H

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STGIPS20C60-H

SLLIMM™ small low-loss intelligent molded module
IPM, 3-phase inverter - 20 A, 600 V short-circuit rugged IGBT

**Applications**
- 3-phase inverters for motor drives
- Air conditioners

**Description**
This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as motor drives and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

**Features**
- IPM 20 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down / pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- DBC leading to low thermal resistance
- Isolation rating of 2500 V rms/min
- UL recognized: UL1557 file E81734

**Table 1. Device summary**

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Packing</th>
</tr>
</thead>
<tbody>
<tr>
<td>STGIPS20C60-H</td>
<td>GIPS20C60-H</td>
<td>SDIP-25L</td>
<td>Tube</td>
</tr>
</tbody>
</table>

This is information on a product in full production.

April 2015

DocID024483 Rev 4
## Contents

1. Internal block diagram and pin configuration .......................... 3

2. Electrical ratings .............................................................. 5
   2.1 Absolute maximum ratings ........................................... 5
   2.2 Thermal data ............................................................. 6

3. Electrical characteristics .................................................. 7
   3.1 Control part ............................................................... 9
   3.2 Waveform definitions ................................................ 11

4. Smart shutdown function .................................................. 12

5. Application information .................................................... 14
   5.1 Recommendations ...................................................... 15

6. Package information ....................................................... 16
   6.1 SDIP-25L package information ...................................... 16
   6.2 Packing information .................................................. 18

7. Revision history ............................................................. 19
1 Internal block diagram and pin configuration

Figure 1. Internal block diagram
Table 2. Pin description

<table>
<thead>
<tr>
<th>Pin n°</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT_U</td>
<td>High-side reference output for U phase</td>
</tr>
<tr>
<td>2</td>
<td>V_{bootU}</td>
<td>Bootstrap voltage for U phase</td>
</tr>
<tr>
<td>3</td>
<td>LIN_U</td>
<td>Low-side logic input for U phase</td>
</tr>
<tr>
<td>4</td>
<td>HIN_U</td>
<td>High-side logic input for U phase</td>
</tr>
<tr>
<td>5</td>
<td>V_{CC}</td>
<td>Low voltage power supply</td>
</tr>
<tr>
<td>6</td>
<td>OUT_V</td>
<td>High-side reference output for V phase</td>
</tr>
<tr>
<td>7</td>
<td>V_{bootV}</td>
<td>Bootstrap voltage for V phase</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>LIN_V</td>
<td>Low-side logic input for V phase</td>
</tr>
<tr>
<td>10</td>
<td>HIN_V</td>
<td>High-side logic input for V phase</td>
</tr>
<tr>
<td>11</td>
<td>OUT_W</td>
<td>High-side reference output for W phase</td>
</tr>
<tr>
<td>12</td>
<td>V_{bootW}</td>
<td>Bootstrap voltage for W phase</td>
</tr>
<tr>
<td>13</td>
<td>LIN_W</td>
<td>Low-side logic input for W phase</td>
</tr>
<tr>
<td>14</td>
<td>HIN_W</td>
<td>High-side logic input for W phase</td>
</tr>
<tr>
<td>15</td>
<td>SD/OD</td>
<td>Shutdown logic input (active low) / open-drain (comparator output)</td>
</tr>
<tr>
<td>16</td>
<td>CIN</td>
<td>Comparator input</td>
</tr>
<tr>
<td>17</td>
<td>N_W</td>
<td>Negative DC input for W phase</td>
</tr>
<tr>
<td>18</td>
<td>W</td>
<td>W phase output</td>
</tr>
<tr>
<td>19</td>
<td>P</td>
<td>Positive DC input</td>
</tr>
<tr>
<td>20</td>
<td>N_V</td>
<td>Negative DC input for V phase</td>
</tr>
<tr>
<td>21</td>
<td>V</td>
<td>V phase output</td>
</tr>
<tr>
<td>22</td>
<td>P</td>
<td>Positive DC input</td>
</tr>
<tr>
<td>23</td>
<td>N_U</td>
<td>Negative DC input for U phase</td>
</tr>
<tr>
<td>24</td>
<td>U</td>
<td>U phase output</td>
</tr>
<tr>
<td>25</td>
<td>P</td>
<td>Positive DC input</td>
</tr>
</tbody>
</table>

Figure 2. Pin layout (bottom view)
STGIPS20C60-H

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{PN})</td>
<td>Supply voltage applied between (P - N_U, N_V, N_W)</td>
<td>450</td>
<td>V</td>
</tr>
<tr>
<td>(V_{PN(surge)})</td>
<td>Supply voltage (surge) applied between (P - N_U, N_V, N_W)</td>
<td>500</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CES})</td>
<td>Each IGBT collector emitter voltage ((V_{IN}^{(1)} = 0))</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>(\pm I_C)</td>
<td>Each IGBT continuous collector current at (T_C = 25^\circ C)</td>
<td>20</td>
<td>A</td>
</tr>
<tr>
<td>(\pm I_{CP}^{(2)})</td>
<td>Each IGBT pulsed collector current</td>
<td>40</td>
<td>A</td>
</tr>
<tr>
<td>(P_{TOT})</td>
<td>Each IGBT total dissipation at (T_C = 25^\circ C)</td>
<td>46</td>
<td>W</td>
</tr>
<tr>
<td>(t_{scw})</td>
<td>Short circuit withstand time, (V_{CE} = 0.5 V_{BRICES}) (T_j = 125^\circ C, V_{CC} = V_{boot} = 15 V, V_{IN}^{(1)} = 0 - 5 V)</td>
<td>5</td>
<td>µs</td>
</tr>
</tbody>
</table>

1. Applied between \(HIN_i, LIN_i\) and \(GND\) for \(i = U, V, W\)
2. Pulse width limited by max junction temperature

Table 4. Control part

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OUT})</td>
<td>Output voltage applied between (OUT_U, OUT_V, OUT_W - GND)</td>
<td>(V_{boot} - 21) to (V_{boot} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CC})</td>
<td>Low voltage power supply</td>
<td>-0.3 to +21</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CIN})</td>
<td>Comparator input voltage</td>
<td>-0.3 to (V_{CC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{boot})</td>
<td>Bootstrap voltage applied between (V_{boot i} - OUT_i) for (i = U, V, W)</td>
<td>-0.3 to 620</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>Logic input voltage applied between (HIN, LIN) and (GND)</td>
<td>-0.3 to 15</td>
<td>V</td>
</tr>
<tr>
<td>(V_{SD/OD})</td>
<td>Open drain voltage</td>
<td>-0.3 to 15</td>
<td>V</td>
</tr>
<tr>
<td>(dV_{OUT}/dt)</td>
<td>Allowed output slew rate</td>
<td>50</td>
<td>V/ns</td>
</tr>
</tbody>
</table>

Table 5. Total system

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{ISO})</td>
<td>Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, (t = 60) sec.)</td>
<td>2500</td>
<td>V</td>
</tr>
<tr>
<td>(T_j)</td>
<td>Power chips operating junction temperature</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>(T_C)</td>
<td>Module case operation temperature</td>
<td>-40 to 125</td>
<td>°C</td>
</tr>
</tbody>
</table>
2.2 Thermal data

Table 6. Thermal data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thJC}$</td>
<td>Thermal resistance junction-case single IGBT</td>
<td>2.7</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>Thermal resistance junction-case single diode</td>
<td>5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1. Simulated curves refer to typical IGBT parameters and maximum $R_{thJC}$. 

Figure 3. Maximum $I_{C(RMS)}$ current vs. switching frequency

Figure 4. Maximum $I_{C(RMS)}$ current vs. $f_{sine}$

1. Simulated curves refer to typical IGBT parameters and maximum $R_{thJC}$. 

3-phase sinusoidal PWM

$V_{ph} = 300$ V, Modulation Index = 0.8,
PP = 0.6, $T_j = 150$ °C, $T_{case} = 60$ °C

$T_c = 80$ °C

$T_c = 100$ °C

$T_{sine} = 60$ Hz

$T_{sine} = 12$ kHz

$T_{sine} = 16$ kHz

$T_{sine} = 20$ kHz
3 Electrical characteristics

$T_J = 25 \, ^\circ\text{C}$ unless otherwise specified.

### Table 7. Inverter part

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE(sat)}$</td>
<td>Collector-emitter saturation voltage</td>
<td>$V_{CC} = V_{boot} = 15 , \text{V}$, $V_{IN}^{(1)} = 0 \div 5 , \text{V}$, $I_C = 20 , \text{A}$</td>
<td>-</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = V_{boot} = 15 , \text{V}$, $V_{IN}^{(1)} = 0 \div 5 , \text{V}$, $I_C = 20 , \text{A}$, $T_J = 125 , ^\circ\text{C}$</td>
<td>-</td>
<td>1.7</td>
</tr>
<tr>
<td>$I_{CES}$</td>
<td>Collector-cut off current ($V_{IN}^{(1)} = 0$ “logic state”)</td>
<td>$V_{CE} = 550 , \text{V}$, $V_{CC} = V_{Boot} = 15 , \text{V}$</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>$V_F$</td>
<td>Diode forward voltage</td>
<td>$V_{IN}^{(1)} = 0$ “logic state”, $I_C = 20 , \text{A}$</td>
<td>-</td>
<td>1.9</td>
</tr>
</tbody>
</table>

#### Inductive load switching time and energy

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td>Turn-on time</td>
<td>$V_{PN} = 300 , \text{V}$, $V_{CC} = V_{boot} = 15 , \text{V}$</td>
<td>-</td>
<td>390</td>
</tr>
<tr>
<td>$t_{(on)}$</td>
<td>Crossover time (on)</td>
<td>$V_{IN}^{(1)} = 0 \div 5 , \text{V}$, $I_C = 20 , \text{A}$</td>
<td>-</td>
<td>170</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-off time</td>
<td>$I_C = 20 , \text{A}$ (see Figure 5)</td>
<td>-</td>
<td>970</td>
</tr>
<tr>
<td>$t_{(off)}$</td>
<td>Crossover time (off)</td>
<td>$I_C = 20 , \text{A}$</td>
<td>-</td>
<td>150</td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>Reverse recovery time</td>
<td></td>
<td>-</td>
<td>284</td>
</tr>
<tr>
<td>$E_{on}$</td>
<td>Turn-on switching losses</td>
<td></td>
<td>-</td>
<td>520</td>
</tr>
<tr>
<td>$E_{off}$</td>
<td>Turn-off switching losses</td>
<td></td>
<td>-</td>
<td>460</td>
</tr>
</tbody>
</table>

1. Applied between $HIN_i$, $LIN_i$ and $GND$ for $i = U, V, W$.

**Note:** $t_{ON}$ and $t_{OFF}$ include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.
Figure 5. Switching time test circuit

Figure 6. Switching time definition

Figure 4 “Switching time definition” refers to HIN, LIN inputs (active high).
### 3.1 Control part

#### Table 8. Low voltage power supply ($V_{CC} = 15$ V unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC_hys}$</td>
<td>$V_{CC}$ UV hysteresis</td>
<td>$V_{CC} = 10$ V</td>
<td>1.2</td>
<td>1.5</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC_THON}$</td>
<td>$V_{CC}$ UV turn ON threshold</td>
<td>$SD/OD = 5$ V; LIN = HIN = 0, $C_{IN} = 0$</td>
<td>11.5</td>
<td>12</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC_THOFF}$</td>
<td>$V_{CC}$ UV turn OFF threshold</td>
<td>$V_{CC} = 15$ V</td>
<td>10</td>
<td>10.5</td>
<td>11</td>
<td>V</td>
</tr>
</tbody>
</table>

| $I_{QCCU}$ | Undervoltage quiescent supply current              | $V_{CC} = 10$ V | 450  | µA   |

| $I_{QCC}$ | Quiescent current                               | $V_{CC} = 15$ V | 3.5  | mA   |

| $V_{ref}$ | Internal comparator (CIN) reference voltage     |                  | 0.5  | 0.54 | 0.58 | V    |

#### Table 9. Bootstrapped voltage ($V_{CC} = 15$ V unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BS_hys}$</td>
<td>$V_{BS}$ UV hysteresis</td>
<td>$V_{BS} &lt; 9$ V</td>
<td>1.2</td>
<td>1.5</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BS_THON}$</td>
<td>$V_{BS}$ UV turn ON threshold</td>
<td>$SD/OD = 5$ V; LIN = 0, $HIN = 5$ V; $C_{IN} = 0$</td>
<td>11.1</td>
<td>11.5</td>
<td>12.1</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BS_THOFF}$</td>
<td>$V_{BS}$ UV turn OFF threshold</td>
<td>$V_{BS} = 15$ V</td>
<td>9.8</td>
<td>10</td>
<td>10.6</td>
<td>V</td>
</tr>
</tbody>
</table>

| $I_{QBSU}$ | Undervoltage $V_{BS}$ quiescent current | $V_{BS} = 15$ V | 70   | 110  | µA   |

| $I_{QBS}$ | $V_{BS}$ quiescent current              | $SD/OD = 5$ V; LIN = 0, $HIN = 5$ V; $C_{IN} = 0$ | 200  | 300  | µA   |

| $R_{DS(on)}$ | Bootstrap driver on resistance          | $LIN= 5$ V; $HIN= 0$ V | 120  | Ω    |

#### Table 10. Logic inputs ($V_{CC} = 15$ V unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{il}$</td>
<td>Low level logic threshold voltage</td>
<td></td>
<td>0.8</td>
<td>1.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ih}$</td>
<td>High level logic threshold voltage</td>
<td></td>
<td>1.9</td>
<td>2.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{HIN_N}$</td>
<td>HI logic “1” input bias current</td>
<td>$HIN = 15$ V</td>
<td>20</td>
<td>40</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{HIN_I}$</td>
<td>HI logic “0” input bias current</td>
<td>$HIN = 0$ V</td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{LIN_N}$</td>
<td>LI logic “1” input bias current</td>
<td>$LIN = 15$ V</td>
<td>20</td>
<td>40</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{LIN_I}$</td>
<td>LI logic “0” input bias current</td>
<td>$LIN = 0$ V</td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SDn}$</td>
<td>SD logic “0” input bias current</td>
<td>$SD = 15$ V</td>
<td>30</td>
<td>120</td>
<td>300</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SDI}$</td>
<td>SD logic “1” input bias current</td>
<td>$SD = 0$ V</td>
<td>3</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$Dt$</td>
<td>Dead time</td>
<td>see Figure 7 and Table 13</td>
<td>1.2</td>
<td></td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

DocID024483 Rev 4 9/20
### Electrical characteristics

#### STGIPS20C60-H

**Table 11. Sense comparator characteristics (V<sub>CC</sub> = 15 V unless otherwise specified)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;i&gt;i&lt;/i&gt;&lt;sub&gt;b&lt;/sub&gt;</td>
<td>Input bias current</td>
<td>&lt;i&gt;V&lt;/i&gt;&lt;sub&gt;CIN&lt;/sub&gt; = 1 V</td>
<td>-</td>
<td>3</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td>&lt;i&gt;V&lt;/i&gt;&lt;sub&gt;ol&lt;/sub&gt;</td>
<td>Open-drain low-level output voltage</td>
<td>&lt;i&gt;I&lt;/i&gt;&lt;sub&gt;od&lt;/sub&gt; = 3 mA</td>
<td>-</td>
<td>0.5</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>&lt;i&gt;t&lt;/i&gt;&lt;sub&gt;td_comp&lt;/sub&gt;</td>
<td>Comparator delay</td>
<td>SD/OD pulled to 5 V through 100 kΩ resistor</td>
<td>-</td>
<td>90</td>
<td>130</td>
<td>ns</td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate</td>
<td>&lt;i&gt;C&lt;/i&gt;&lt;sub&gt;L&lt;/sub&gt; = 180 pF; &lt;i&gt;R&lt;/i&gt;&lt;sub&gt;pu&lt;/sub&gt; = 5 kΩ</td>
<td>-</td>
<td>60</td>
<td>-</td>
<td>V/µsec</td>
</tr>
<tr>
<td>&lt;i&gt;t&lt;/i&gt;&lt;sub&gt;sd&lt;/sub&gt;</td>
<td>Shut down to high / low side driver propagation delay</td>
<td>&lt;i&gt;V&lt;/i&gt;&lt;sub&gt;OUT&lt;/sub&gt; = 0, &lt;i&gt;V&lt;/i&gt;&lt;sub&gt;Boot&lt;/sub&gt; = &lt;i&gt;V&lt;/i&gt;&lt;sub&gt;CC&lt;/sub&gt;, &lt;i&gt;V&lt;/i&gt;&lt;sub&gt;I&lt;/sub&gt; = 0 to 3.3 V</td>
<td>50</td>
<td>125</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>&lt;i&gt;t&lt;/i&gt;&lt;sub&gt;isd&lt;/sub&gt;</td>
<td>Comparator triggering to high / low side driver turn-off propagation delay</td>
<td>Measured applying a voltage step from 0 V to 3.3 V to pin &lt;i&gt;CIN&lt;/i&gt;</td>
<td>50</td>
<td>200</td>
<td>250</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Table 12. Truth table**

<table>
<thead>
<tr>
<th>Condition</th>
<th>SD/OD</th>
<th>LIN</th>
<th>HIN</th>
<th>LVG</th>
<th>HVG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shutdown enable half-bridge tri-state</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Interlocking half-bridge tri-state</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>0 “logic state” half-bridge tri-state</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>1 “logic state” low side direct driving</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>1 “logic state” high side direct driving</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

**Note:** X: don’t care
3.2 Waveform definitions

Figure 7. Dead time and interlocking waveforms definition

- **CONTROL SIGNAL EDGES OVERLAPPED: INTERLOCKING + DEAD TIME**
  - L/N
  - H/N
  - L/VG
  - H/VG
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)

- **CONTROL SIGNALS EDGES SYNCHRONOUS (**): DEAD TIME**
  - L/N
  - H/N
  - L/VG
  - H/VG
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)

- **CONTROL SIGNALS EDGES NOT OVERLAPPED, BUT INSIDE THE DEAD TIME: DEAD TIME**
  - L/N
  - H/N
  - L/VG
  - H/VG
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)

- **CONTROL SIGNALS EDGES NOT OVERLAPPED, OUTSIDE THE DEAD TIME: DIRECT DRIVING**
  - L/N
  - H/N
  - L/VG
  - H/VG
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)
  - Gate driver outputs OFF (HALF-BRIDGE TRI-STATE)
4 Smart shutdown function

The STGIPS20C60-H integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference $V_{\text{ref}}$ connected to the inverting input, while the non-inverting input, available on pin (CIN), can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the halfbridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the DMOS connected to the open-drain output (pin $\overline{SD}/OD$) is turned on by the internal logic which holds it on until the shutdown voltage is lower than the logic input lower threshold ($V_{il}$). Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.
**Smart shutdown function**

Figure 8. Smart shutdown timing waveforms

An approximation of the disable time is given by:

\[
\tau_1 \approx \tau_1 \cdot \ln\left( \frac{V_{\text{off}} - V_{\text{on}}}{V_{\text{dd}} - V_{\text{on}}} \right)
\]

\[
\tau_2 \approx \tau_2 \cdot \ln\left( \frac{V_{\text{th}} - V_{\text{off}}}{V_{\text{dd}} - V_{\text{off}}} \right)
\]

where:

\[
\tau_1 = \frac{R_{\text{oh,od}}}{R_{\text{sd}}} \cdot C_{\text{sd}}
\]

\[
\tau_2 = \frac{R_{\text{rd,od}} + R_{\text{sd}}}{R_{\text{sd}}} \cdot C_{\text{sd}}
\]

\[
V_{\text{on}} = \frac{R_{\text{oh,od}}}{R_{\text{oh,od}} + R_{\text{sd}}} \cdot V_{\text{bias}}
\]

\[
V_{\text{off}} = \frac{R_{\text{rd,od}}}{R_{\text{rd,od}} + R_{\text{sd}}} \cdot V_{\text{bias}}
\]

Please refer to Table 11 for internal propagation delay time details.
5 Application information

Figure 9. Typical application circuit
5.1 Recommendations

- Input signals HIN, LIN are active high logic. A 375 kΩ (typ.) pull down resistor is built-in for each input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The SD/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see Section 4: Smart shutdown function for detailed info).

Table 13. Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{PN}</td>
<td>Supply Voltage</td>
<td>Applied between P-Nu,Nv,Nw</td>
<td>Min. 300 Typ. 400 Max. V</td>
<td></td>
</tr>
<tr>
<td>V_{CC}</td>
<td>Control supply voltage</td>
<td>Applied between V_{CC}-GND</td>
<td>Min. 13 Typ. 15 Max. 18 V</td>
<td></td>
</tr>
<tr>
<td>V_{BS}</td>
<td>High side bias voltage</td>
<td>Applied between V_{BOOT}-OUT_i for i=U,V,W</td>
<td>Min. 13 Typ. 18 V</td>
<td></td>
</tr>
<tr>
<td>t_{dead}</td>
<td>Blanking time to prevent Arm-short</td>
<td>For each input signal</td>
<td>Min. 1.5 Typ. µs</td>
<td></td>
</tr>
<tr>
<td>f_{PWM}</td>
<td>PWM input signal</td>
<td>-40°C &lt; T_c &lt; 100°C -40°C &lt; T_j &lt; 125°C</td>
<td>Min. 20 Typ. kHz</td>
<td></td>
</tr>
<tr>
<td>T_C</td>
<td>Case operation temperature</td>
<td></td>
<td>Min. 100 Typ. °C</td>
<td></td>
</tr>
</tbody>
</table>

Note: For further details refer to AN3338.
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

6.1 SDIP-25L package information

Figure 10. SDIP-25L package outline
### Table 14. SDIP-25L mechanical data

<table>
<thead>
<tr>
<th>Dim.</th>
<th>mm</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
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<td>A</td>
<td></td>
<td>43.90</td>
<td>44.40</td>
<td>44.90</td>
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<tr>
<td>A2</td>
<td></td>
<td>1.40</td>
<td>1.60</td>
<td>1.80</td>
</tr>
<tr>
<td>A3</td>
<td></td>
<td>38.90</td>
<td>39.40</td>
<td>39.90</td>
</tr>
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<td>B</td>
<td></td>
<td>21.50</td>
<td>22.00</td>
<td>22.50</td>
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<tr>
<td>B1</td>
<td></td>
<td>11.25</td>
<td>11.85</td>
<td>12.45</td>
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<tr>
<td>B2</td>
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<td>25.23</td>
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<tr>
<td>C</td>
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</tr>
<tr>
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<td>3.10</td>
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<td>e</td>
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</tr>
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<td></td>
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<td></td>
<td></td>
</tr>
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<tr>
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<td></td>
<td>0.35</td>
<td>0.50</td>
<td>0.65</td>
</tr>
<tr>
<td>R</td>
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<td>1.75</td>
<td>1.95</td>
</tr>
<tr>
<td>T</td>
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<td>0.45</td>
<td>0.55</td>
<td>0.65</td>
</tr>
<tr>
<td>V</td>
<td></td>
<td>0°</td>
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<td>6°</td>
</tr>
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</table>
6.2 Packing information

Figure 11. SDIP-25L packing information

Base quantity: 11 pcs
Bulk quantity: 133 pcs
7 Revision history

Table 15. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tbody>
<tr>
<td>09-Apr-2013</td>
<td>1</td>
<td>Initial release</td>
</tr>
<tr>
<td>08-Jul-2013</td>
<td>2</td>
<td>Updated $V_F$ typ value in Table 7: Inverter part and $D_t$ value in Table 10: Logic inputs ($VCC = 15 V$ unless otherwise specified).</td>
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<tr>
<td>14-May-2014</td>
<td>3</td>
<td>Document status promoted from preliminary to production data. Updated Table 3: Inverter part, Table 6: Thermal data, Table 7: Inverter part and Section 6.2: Packing information. Minor text changes.</td>
</tr>
<tr>
<td>10-Apr-2015</td>
<td>4</td>
<td>Minor text edits throughout document Updated Figure 2: Pin layout (bottom view) Updated Section 6: Package information</td>
</tr>
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</table>