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CTLDM3590

**SURFACE MOUNT
N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**



Top View Bottom View

TLM3D6D8 CASE



www.centrasemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM3590 is an enhancement-mode N-channel MOSFET designed for applications including high speed pulsed amplifiers and drivers. This MOSFET has beneficially low $r_{DS(ON)}$, low threshold voltage, and very low gate charge characteristics.

MARKING CODE: 1

FEATURES:

- ESD protection up to 2kV
- Power dissipation: 125mW
- Low $r_{DS(ON)}$
- Low threshold voltage
- Ultra small, ultra low profile 0.6mm x 0.8mm x 0.4mm TLM™ leadless surface mount package

APPLICATIONS:

- Load/Power Switches
- Boost/Buck Converters
- Battery Charging/Power Management

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage
Gate-Source Voltage
Continuous Drain Current (Steady State)
Pulsed Drain Current, $t_p=10\mu\text{s}$
Power Dissipation
Operating and Storage Junction Temperature
Thermal Resistance

SYMBOL

V_{DS}	20
V_{GS}	8.0
I_D	160
I_D	800
P_D	125
T_J, T_{stg}	-65 to +150
θ_{JA}	1000

UNITS

V
V
mA
mA
mW
°C
°C/W

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

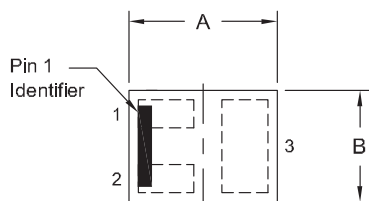
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=5.0V, V_{DS}=0$			100	nA
I_{DSS}	$V_{DS}=5.0V, V_{GS}=0$			50	nA
I_{DSS}	$V_{DS}=16V, V_{GS}=0$			100	nA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	20			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.4		1.0	V
$r_{DS(ON)}$	$V_{GS}=4.5V, I_D=100\text{mA}$		1.5	3.0	Ω
$r_{DS(ON)}$	$V_{GS}=2.5V, I_D=50\text{mA}$		2.0	4.0	Ω
$r_{DS(ON)}$	$V_{GS}=1.8V, I_D=20\text{mA}$		3.0	6.0	Ω
$r_{DS(ON)}$	$V_{GS}=1.5V, I_D=10\text{mA}$		4.0	10	Ω
$r_{DS(ON)}$	$V_{GS}=1.2V, I_D=1.0\text{mA}$		7.0		Ω
$Q_{g(tot)}$	$V_{DS}=10V, V_{GS}=4.5V, I_D=100\text{mA}$		0.458		nC
Q_{gs}	$V_{DS}=10V, V_{GS}=4.5V, I_D=100\text{mA}$		0.176		nC
Q_{gd}	$V_{DS}=10V, V_{GS}=4.5V, I_D=100\text{mA}$		0.138		nC
g_{FS}	$V_{DS}=5.0V, I_D=125\text{mA}$		1.3		S
C_{rss}	$V_{DS}=15V, V_{GS}=0, f=1.0\text{MHz}$		2.2		pF
C_{iss}	$V_{DS}=15V, V_{GS}=0, f=1.0\text{MHz}$		9.0		pF
C_{oss}	$V_{DS}=15V, V_{GS}=0, f=1.0\text{MHz}$		3.0		pF
t_{on}	$V_{DD}=10V, V_{GS}=4.5V, I_D=200\text{mA}$		25		ns
t_{off}	$V_{DD}=10V, V_{GS}=4.5V, I_D=200\text{mA}$		85		ns

R3 (27-September 2012)

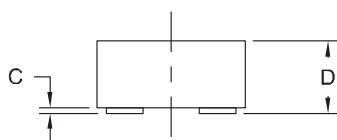
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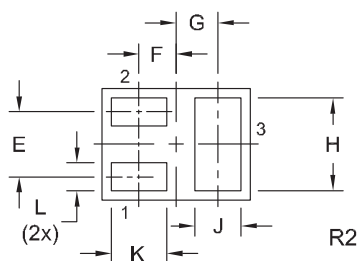
TLM3D6D8 CASE - MECHANICAL OUTLINE



TOP VIEW



SIDE VIEW

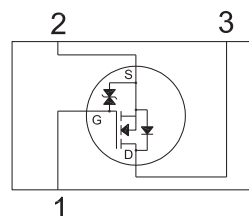


BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.029	0.034	0.75	0.85
B	0.021	0.026	0.55	0.65
C	0.000	0.002	0.00	0.05
D	0.012	0.016	0.31	0.40
E	0.014		0.35	
F	0.008		0.20	
G	0.009		0.225	
H	0.017	0.022	0.45	0.55
J	0.008	0.012	0.20	0.30
K	0.010	0.014	0.25	0.35
L	0.004	0.008	0.10	0.20

TLM3D6D8 (REV: R2)

PIN CONFIGURATION
(Bottom View)



LEAD CODE:

- 1) Gate
- 2) Source
- 3) Drain

MARKING CODE: 1

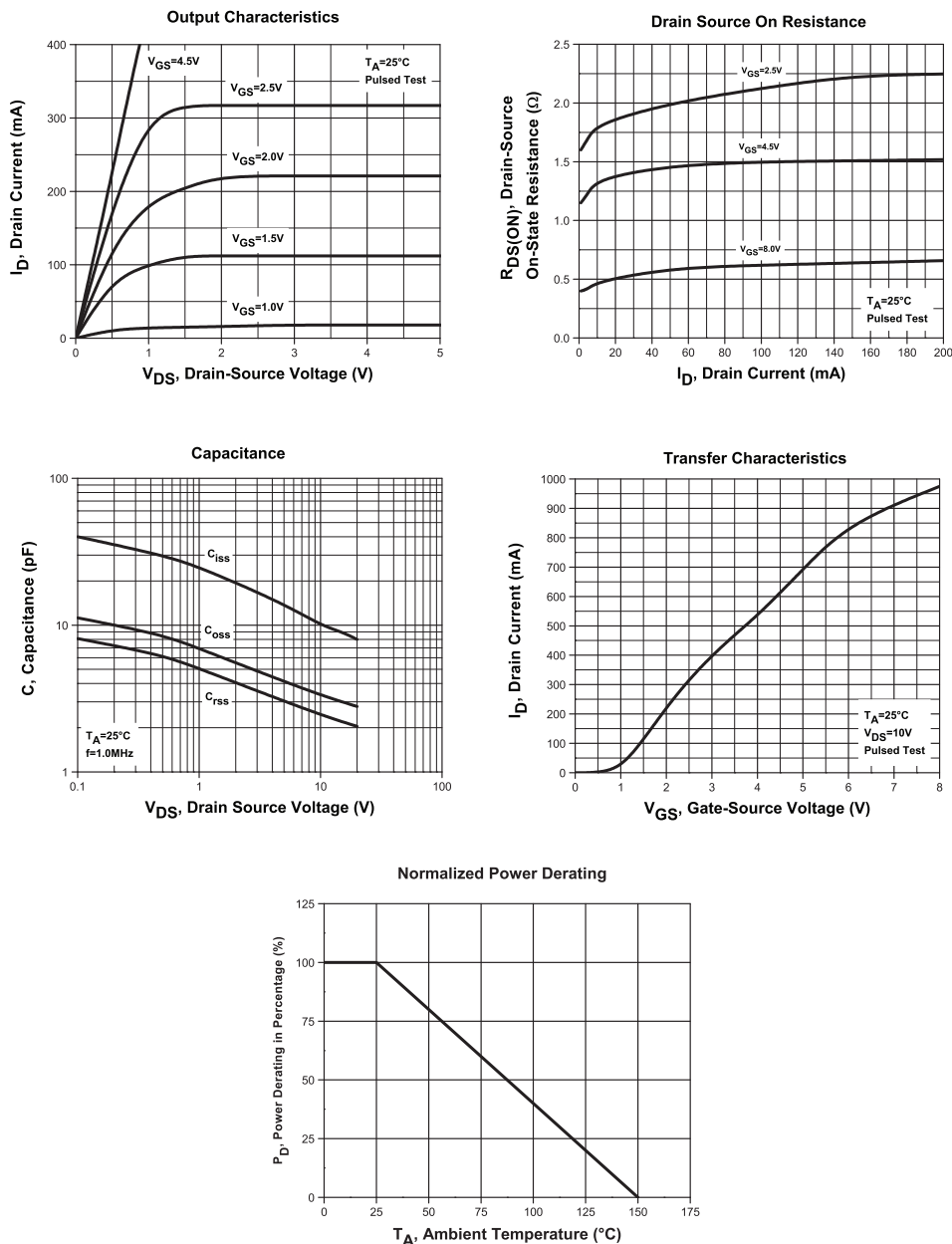
R3 (27-September 2012)

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TYPICAL ELECTRICAL CHARACTERISTICS



R3 (27-September 2012)

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PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:

www.centrasemi.com/wwreps

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