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Texas Instruments
AM26LV31EIDR

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Datasheet of AM26LV31EIDR - IC DRIVER DIFF QUAD LV HS 16SOIC
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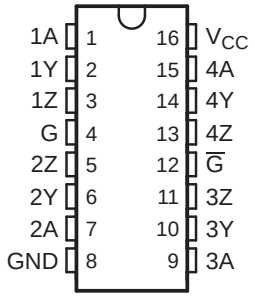
LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE DRIVER WITH ±15-kV IEC ESD PROTECTION

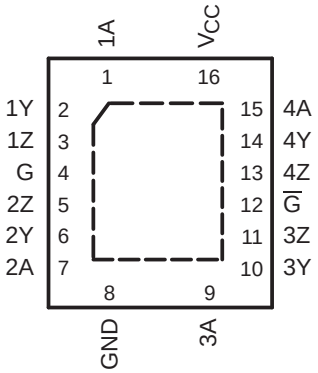
FEATURES

- **Meets or Exceeds Standards TIA/EIA-422-B and ITU Recommendation V.11**
- **Operates From a Single 3.3-V Power Supply**
- **ESD Protection for RS422 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC61000-4-2, Contact Discharge**
  - **±15-kV IEC61000-4-2, Air-Gap Discharge**
- **Switching Rates up to 32 MHz**
- **Propagation Delay Time . . . 8 ns Typ**
- **Pulse Skew Time . . . 500 ps Typ**
- **High Output-Drive Current . . . ±30 mA**
- **Controlled Rise and Fall Times . . . 5 ns Typ**
- **Differential Output Voltage With 100-Ω Load . . . 2.6 V Typ**
- **Accepts 5-V Logic Inputs With 3.3-V Supply**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Driver Output Short-Protection Circuit**
- **Glitch-Free Power-Up/Power-Down Protection**
- **Package Options: SOP, SOIC, TSSOP, QFN**

D, NS, OR PW PACKAGE (TOP VIEW)



RGY PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The AM26LV31E is a quadruple differential line driver with 3-state outputs. This driver has ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection. This device is designed to meet TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply voltage.

The device is optimized for balanced-bus transmission at switching rates up to 32 MHz. The outputs have high current capability for driving balanced lines, such as twisted-pair transmission lines, and provide a high impedance in the power-off condition.

The AM26LV31EI is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tape and reel	AM26LV31EIDR	AM26LV3IEI
	SOP – NS	Tape and reel	AM26LV31EINSR	26LV31EI
	TSSOP – PW	Tape and reel	AM26LV31EIPWR	SB31
	QFN – RGY	Tape and reel	AM26LV31EIRGYR	SB31

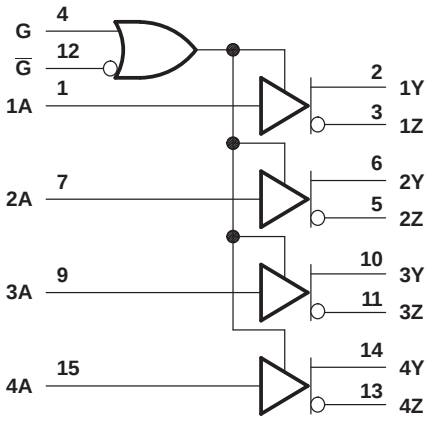
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE(1)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

LOGIC DIAGRAM



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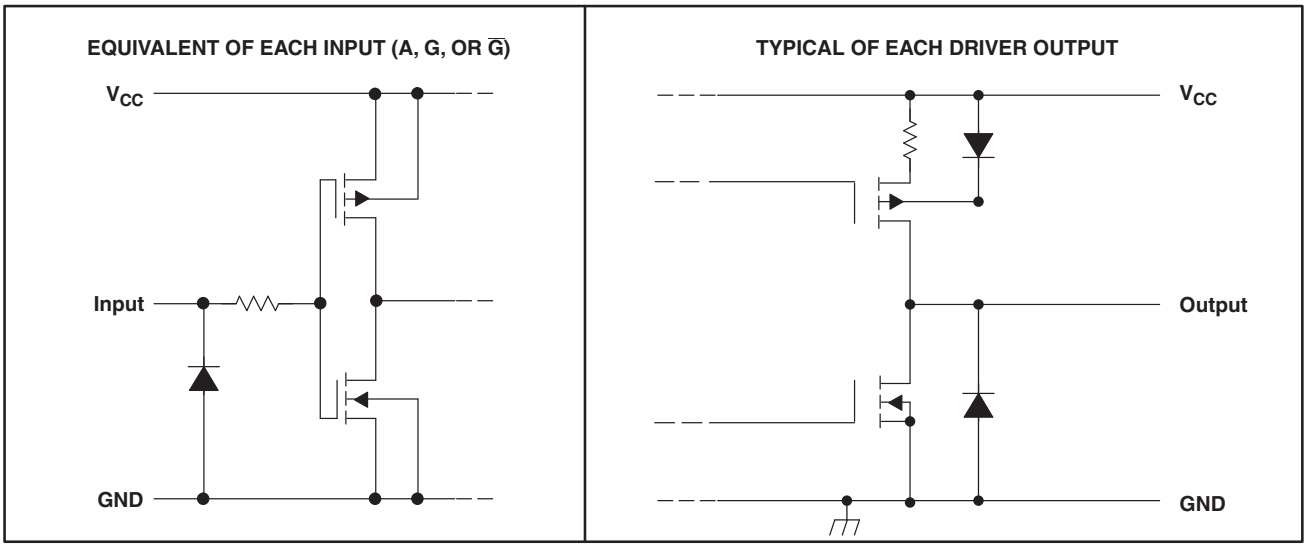
SCHEMATIC



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		–0.5	6	V
V_I	Input voltage range		–0.5	6	V
V_O	Output voltage range		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_O	Continuous output current			±150	mA
	Continuous current through V_{CC} or GND			±200	mA
T_J	Operating virtual junction temperature			150	°C
θ_{JA}	Package thermal impedance[3][4]	D package		73	°C/W
		NS package		64	
		PW package		108	
		RGY package		39	
T_A	Operating free-air temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.
(3) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage	0		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–30	mA
I_{OL}	Low-level output current			30	mA
T_A	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –20 mA	2.4	3		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.2	0.4	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0 mA	2		4	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω (see Figure 1)(2)	2	2.6		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 100 Ω (see Figure 1)(2)			±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100 Ω (see Figure 1)(2)		1.5	2	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage	R_L = 100 Ω (see Figure 1)(2)			±0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0, V_O = –0.25 V or 5.5 V			±100	µA
I_{OZ}	High-impedance state output current	V_O = –0.25 V or 5.5 V, G = 0.8 V or $\overline{G}$ = 2 V			±100	µA
I_I	Input current	V_{CC} = 0 or 3.6 V, V_I = 0 or 5.5 V			±10	µA
I_{OS}	Short-circuit output current	V_O = V_{CC} or GND(3)	–30		–150	mA
I_{CC}	Supply current (total package)	V_I = V_{CC} or GND, No load, enable			100	µA
C_{pd}	Power dissipation capacitance	No load(4)		160		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Refer to TIA-EIA-422-B for exact conditions.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

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SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 2	4	8	12	ns
t_{PLH}	Propagation delay time, low- to high-level output		4	8	12	ns
t_t	Transition time (t_r or t_f)	See Figure 2		5	10	ns
t_{PZH}	Output-enable time to high level	See Figure 3		10	20	ns
t_{PZL}	Output-enable time to low level	See Figure 4		10	20	ns
t_{PHZ}	Output-disable time from high level	See Figure 3		10	20	ns
t_{PLZ}	Output-disable time from low level	See Figure 4		10	20	ns
$t_{sk(p)}$	Pulse skew	See Figure 2(2)(3)		0.5	1.5	ns
$t_{sk(o)}$	Skew limit (pin to pin)				1.5	ns
$t_{sk(lim)}$	Skew limit (device to device)				3	ns
$f_{(max)}$	Maximum operating frequency	See Figure 2		32		MHz

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver output	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

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PARAMETER MEASUREMENT INFORMATION

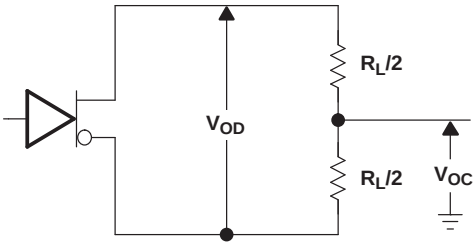
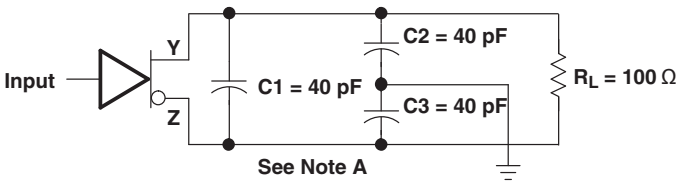
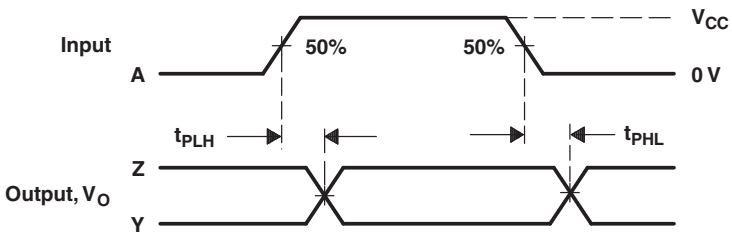
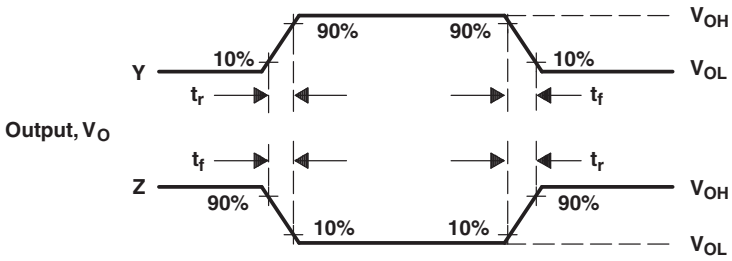


Figure 1. Test Circuit, V_{OD} and V_{OC}





PROPAGATION DELAY TIMES



RISE AND FALL TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, 50% duty cycle, t_r and t_f ≤ 2 ns.

Figure 2. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

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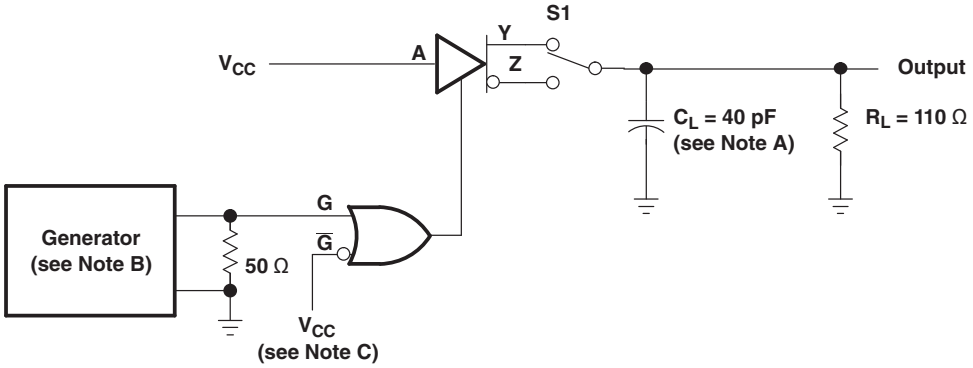
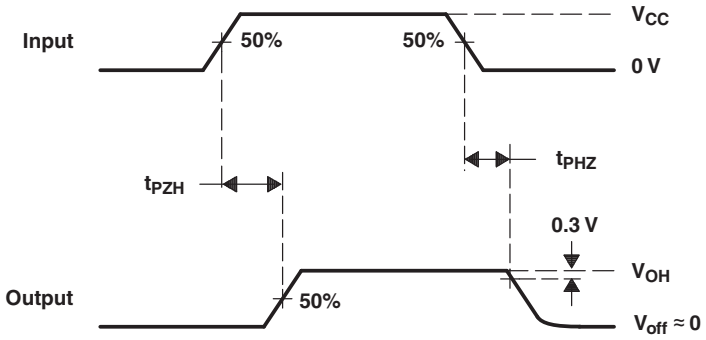
PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT

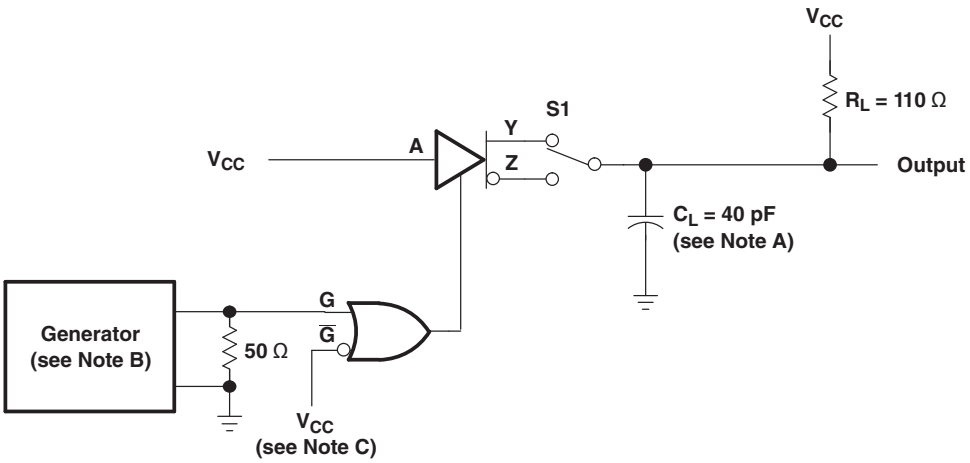


VOLTAGE WAVEFORMS

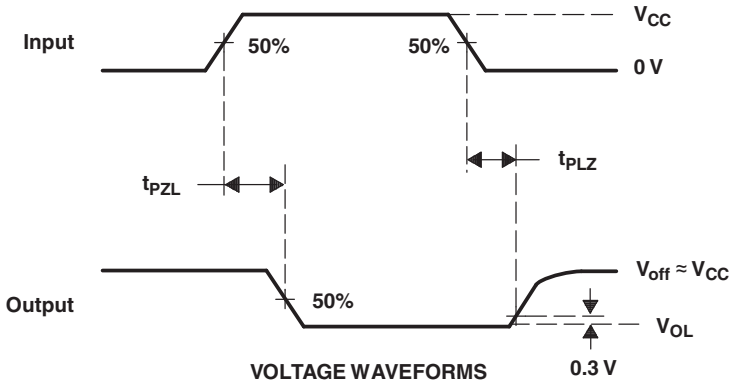
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r and t_f ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r and t_f ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV31EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI	Samples
AM26LV31EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV31EI	Samples
AM26LV31EINSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV31EI	Samples
AM26LV31EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	Samples
AM26LV31EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SB31	Samples
AM26LV31EIRGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SB31	Samples
AM26LV31EIRGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SB31	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF AM26LV31E :

- Enhanced Product: AM26LV31E-EP

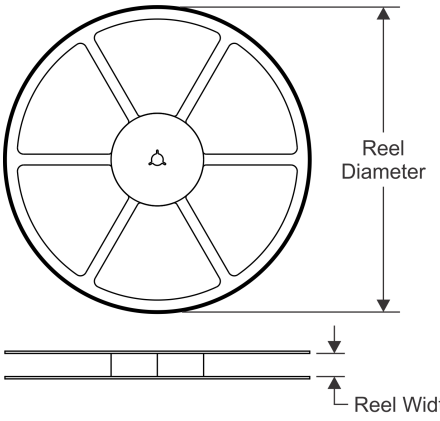
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

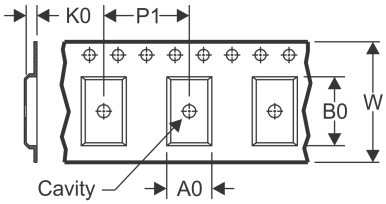
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

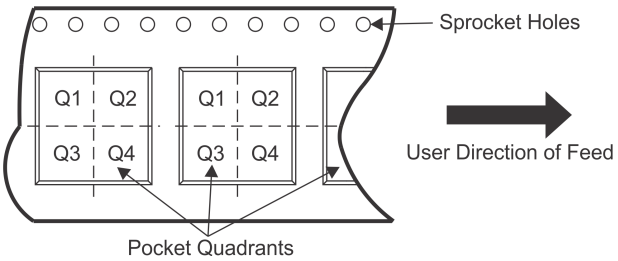


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



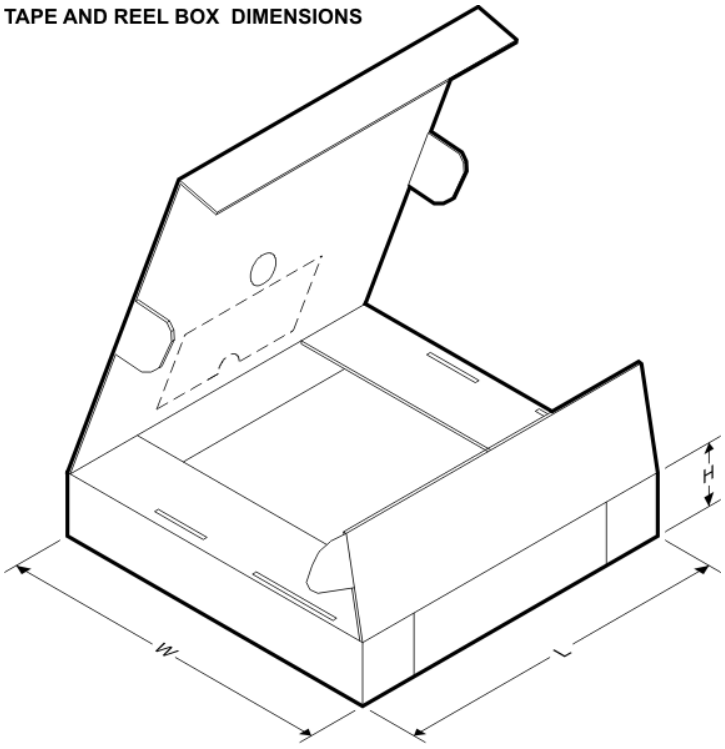
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26LV31EIRGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 26-Mar-2016

TAPE AND REEL BOX DIMENSIONS

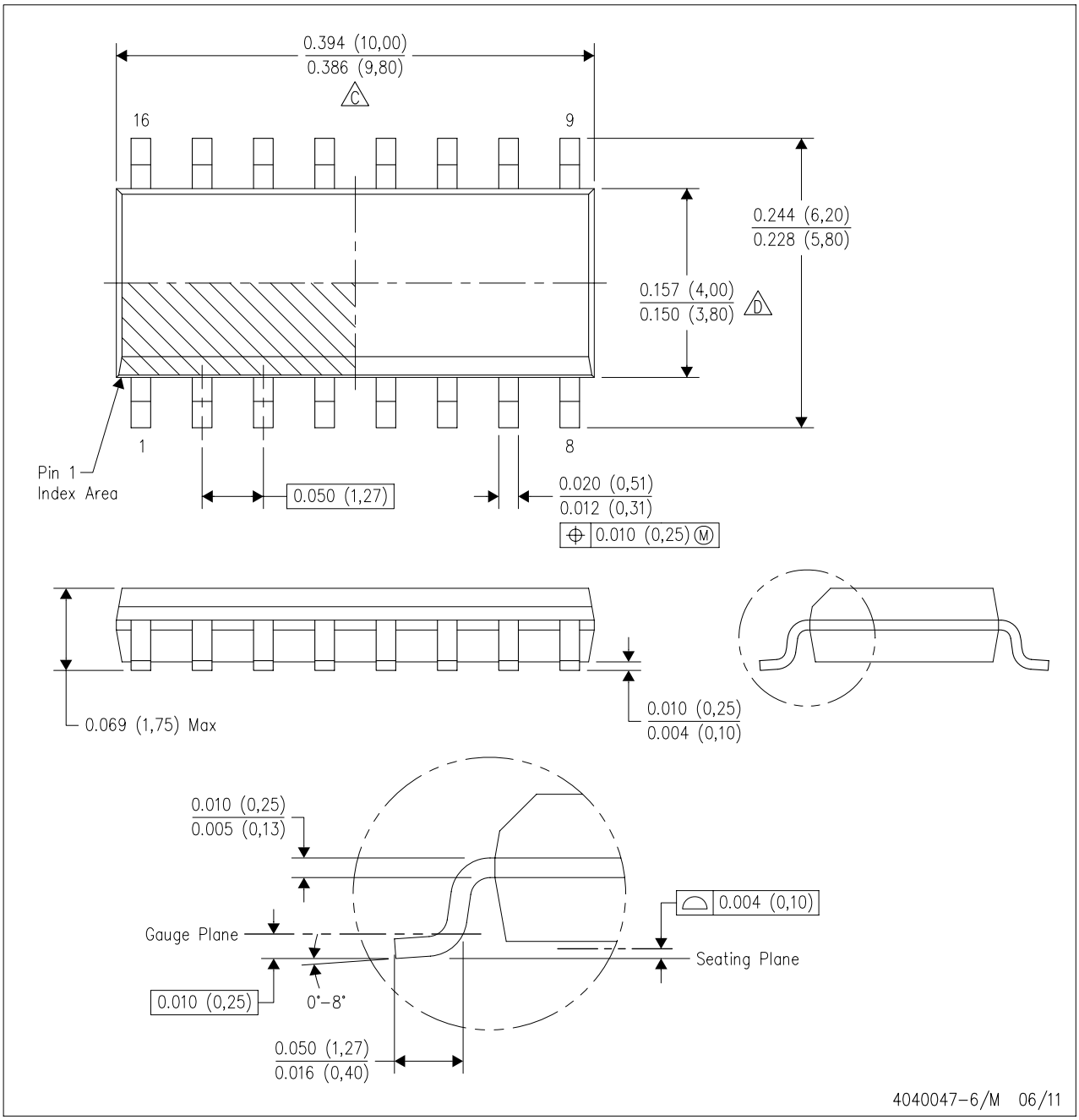


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31EIDR	SOIC	D	16	2500	367.0	367.0	38.0
AM26LV31EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26LV31EIRGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

MECHANICAL DATA

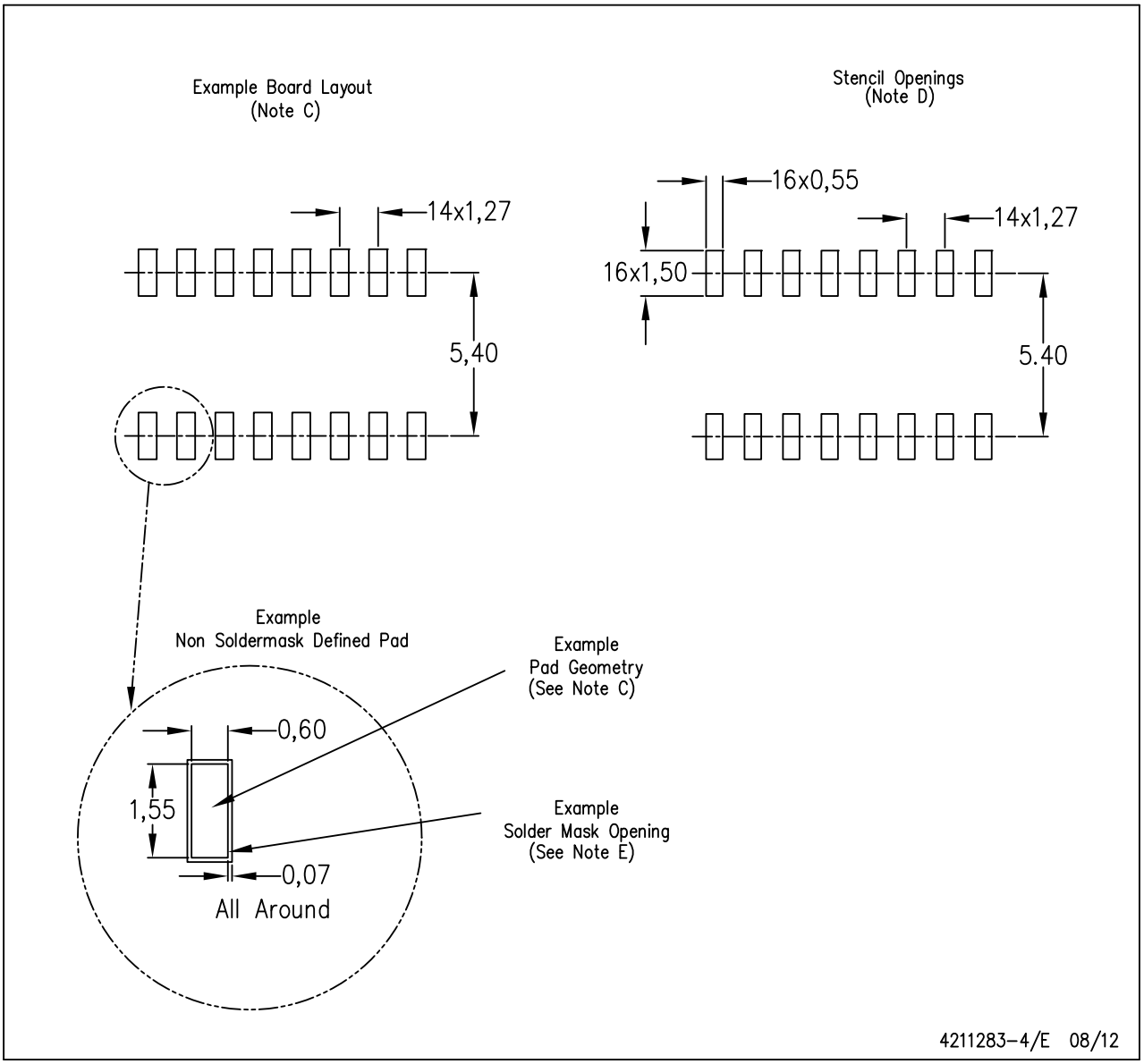
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

LAND PATTERN DATA

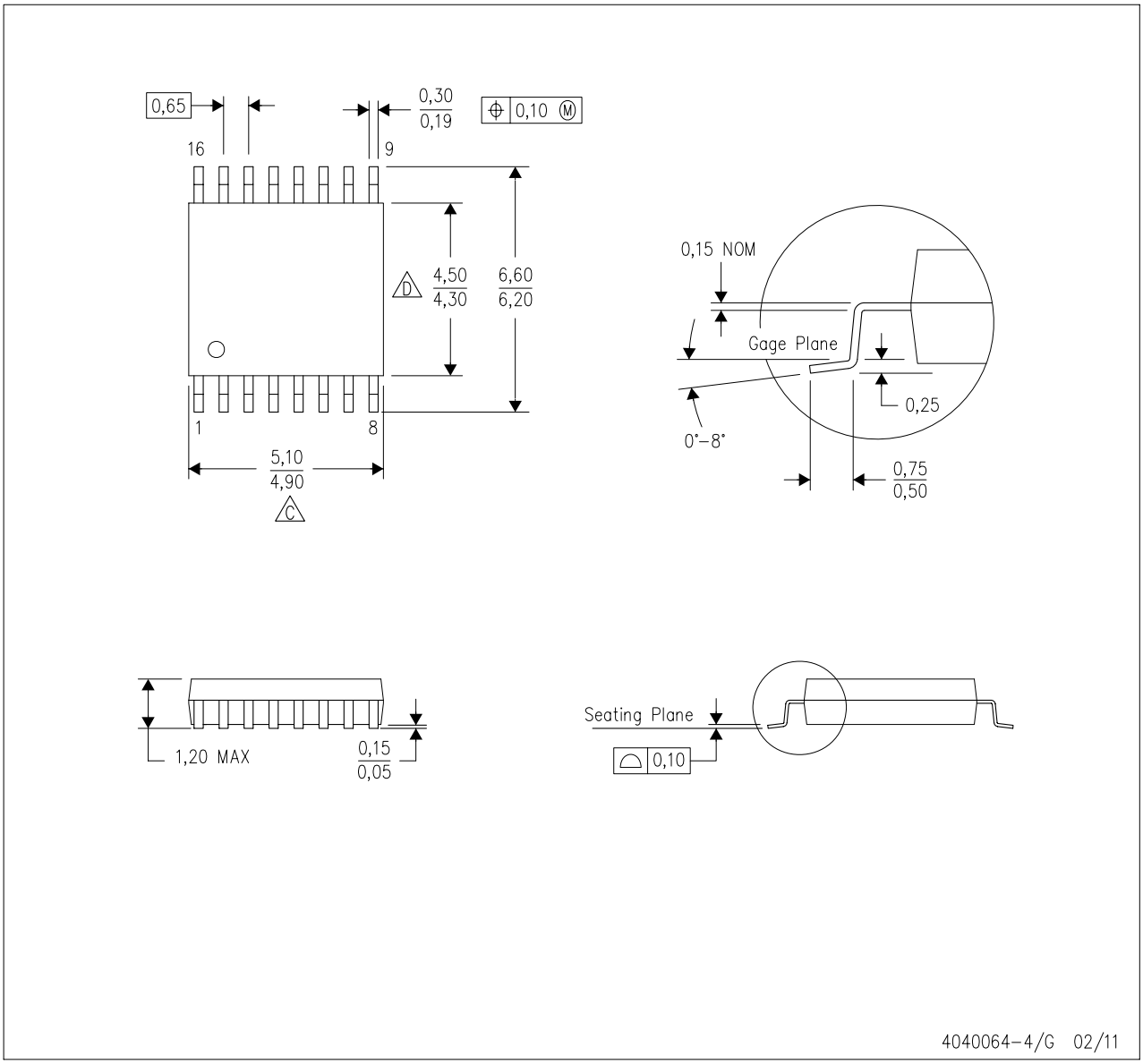
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

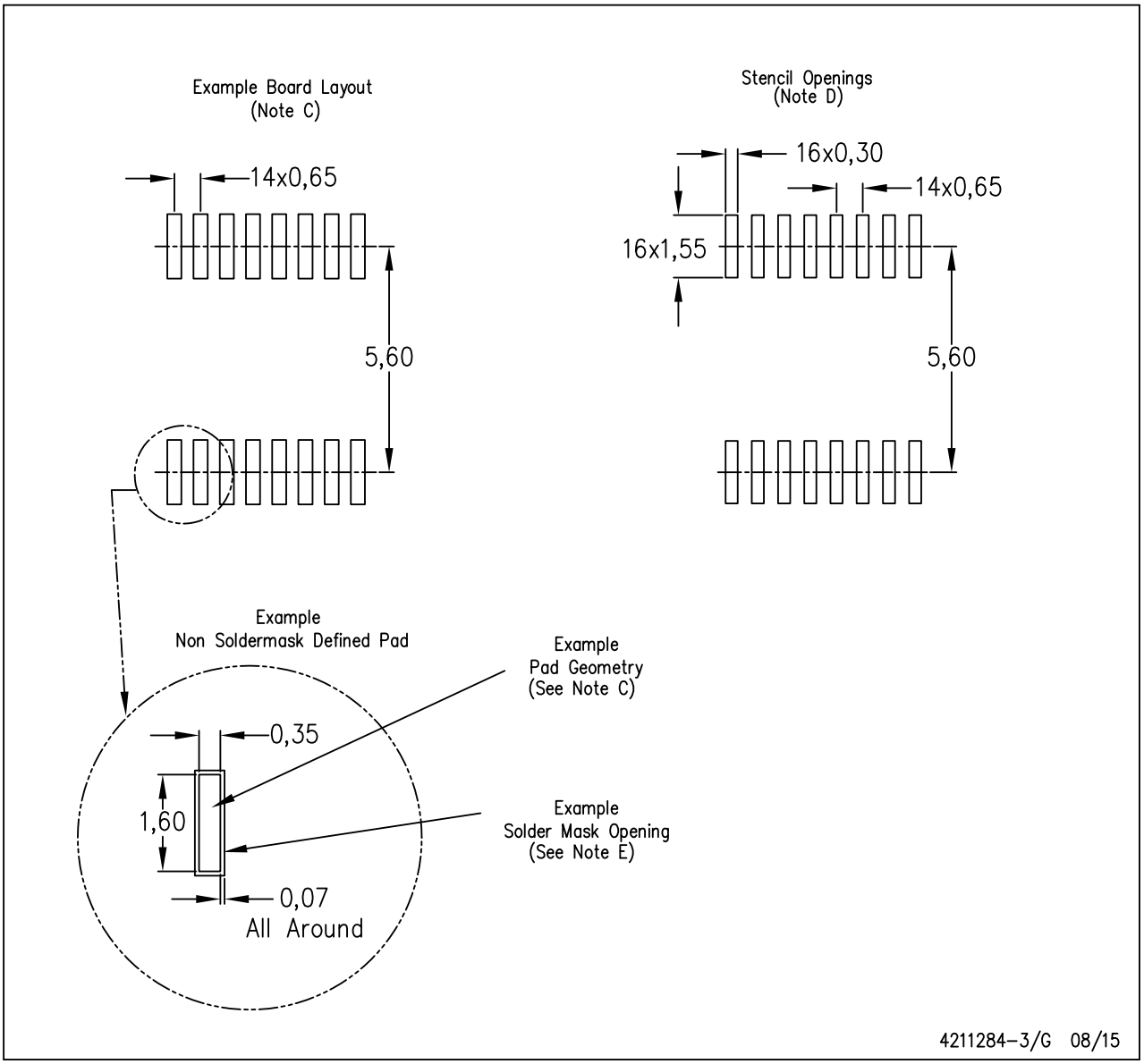
PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

LAND PATTERN DATA

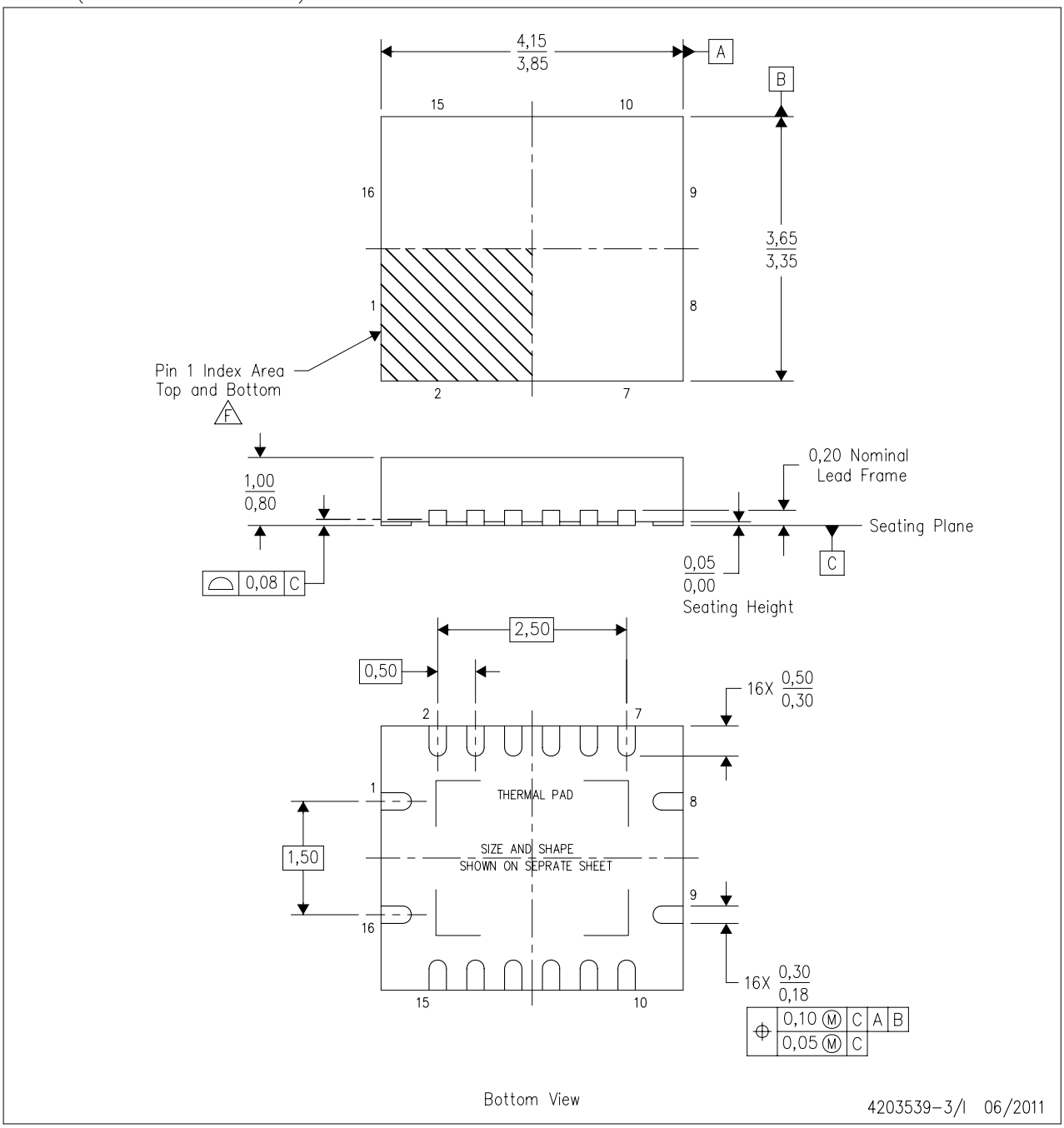
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.

THERMAL PAD MECHANICAL DATA

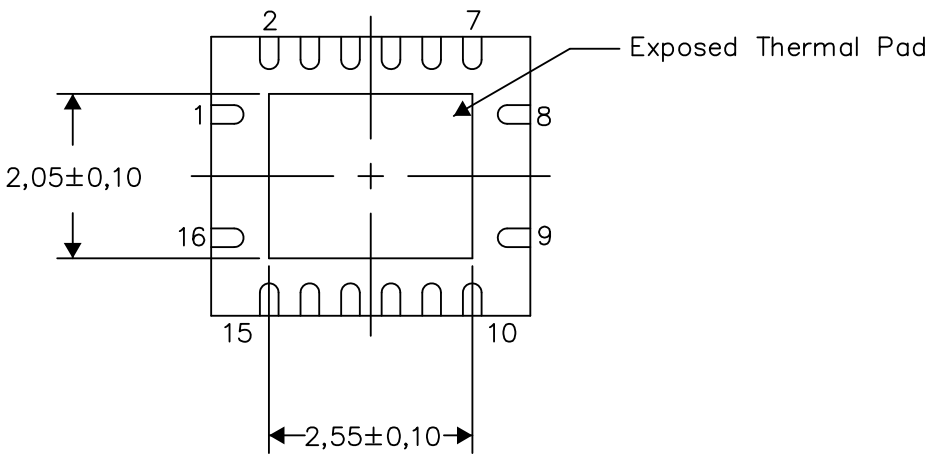
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

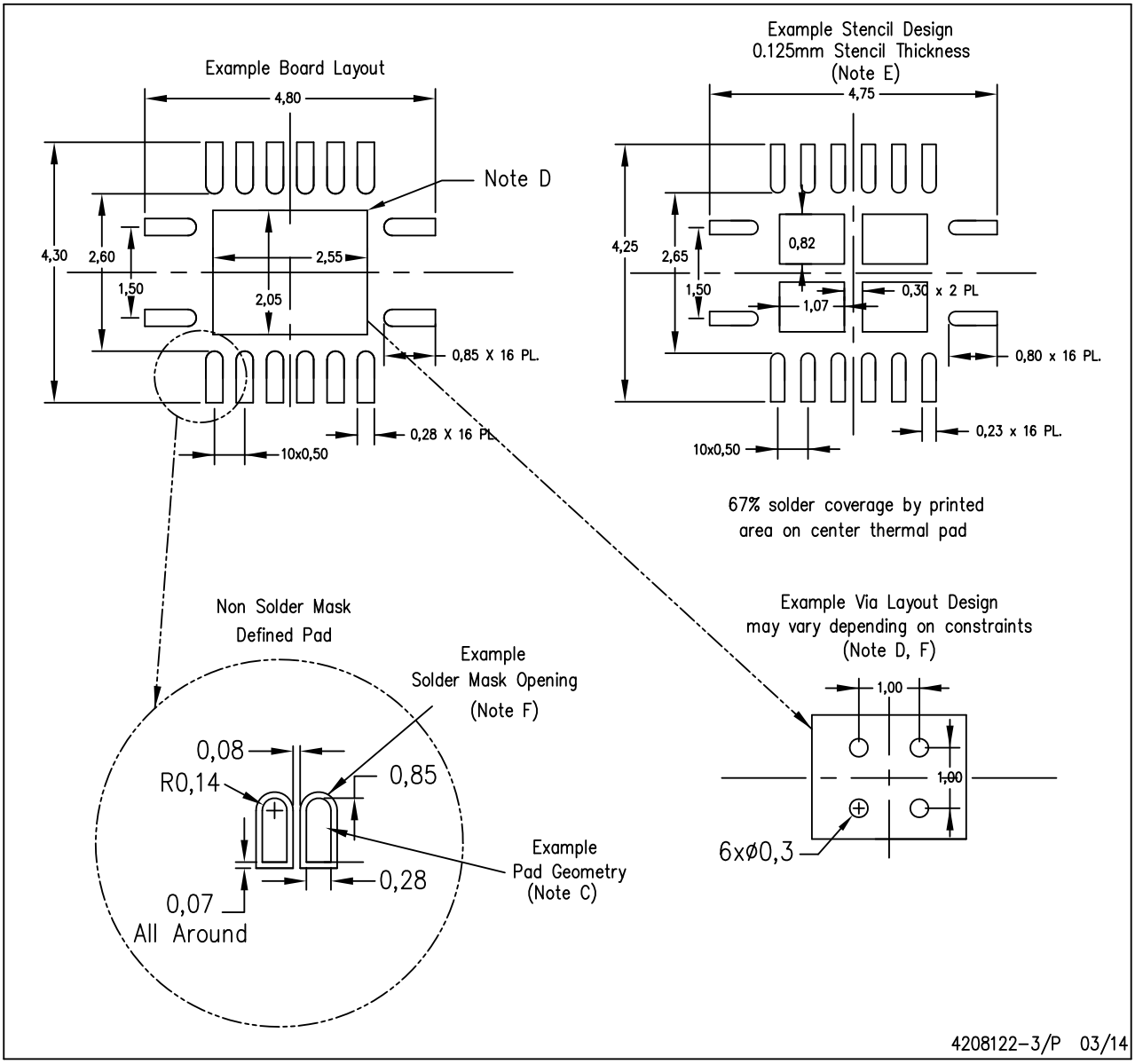
Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

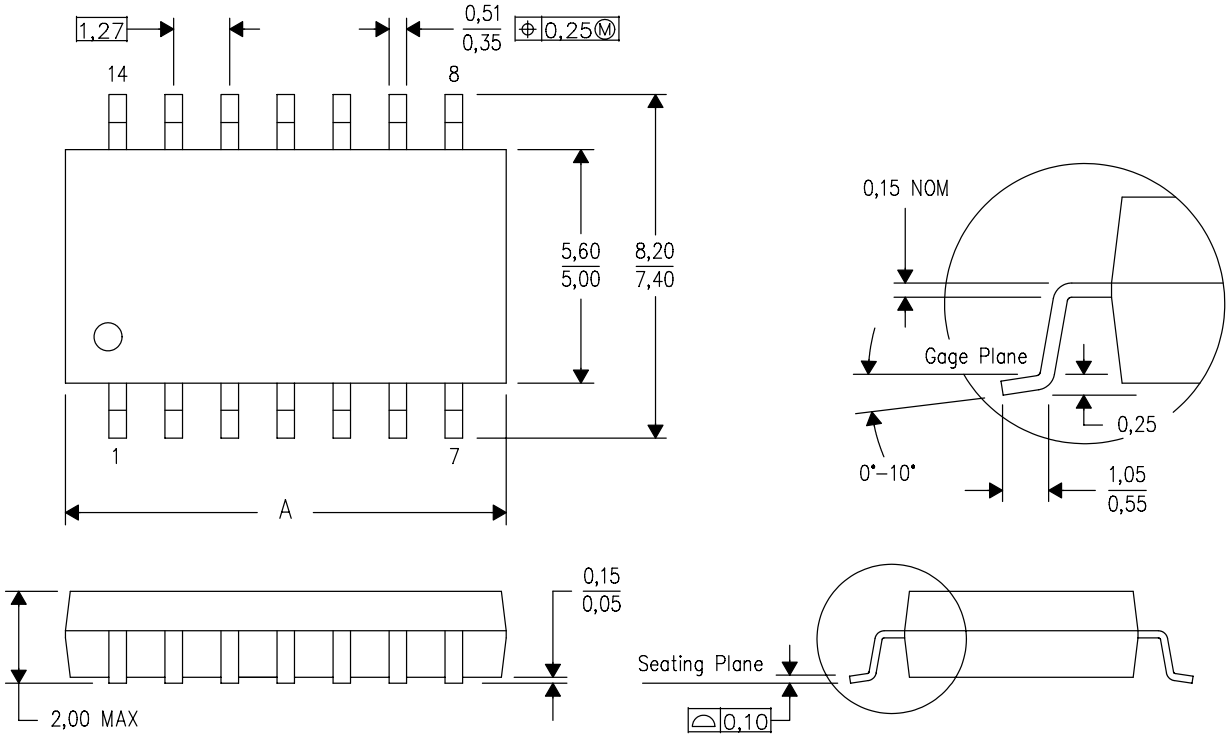


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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