Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Maxim Integrated
MAX9381ESA+

For any questions, you can email us directly:
sales@integrated-circuit.com
General Description
The MAX9381 differential data, differential clock D flip-flop is pin compatible with the ON Semiconductor MC100EP52, with the added benefit of a wider supply voltage range from 2.25V to 5.5V and 25% lower supply current. Data enters the master part of the flip-flop when the clock is low and is transferred to the outputs upon a positive transition of the clock. Interchanging the clock inputs allows the part to be used as a negative edge-triggered device. The MAX9381 utilizes input clamping circuits that ensure the stability of the outputs when the inputs are left open or at VEE.

The MAX9381 is offered in an 8-pin SO package and the smaller 8-pin µMAX package.

Features
- 3.0GHz Guaranteed Operating Clock Frequency
- 0.2ps RMS Added Random Jitter
- 328ps Typical Propagation Delay
- PECL Operation from VCC = 2.25V to 5.5V with VEE = 0V
- ECL Operation from VEE = -2.25V to -5.5V with VCC = 0V
- Input Safety Clamps Ensure Output Stability when Inputs are Open or at VEE
- ±2kV ESD Protection (Human Body Model)

Applications
- Precision Clock and Data Distribution
- Central Office
- DSLAM
- DLC
- Base Station
- ATE

Functional Diagram

Pin Configuration

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim’s website at www.maxim-ic.com.
**Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop**

### ABSOLUTE MAXIMUM RATINGS

- **VCC - VEE**: -0.3V to +6.0V
- **Input Voltage (D, D, CLK, CLK)**: (VEE - 0.3V) to (VCC + 3V)
- **Differential Input Voltage**: Smaller of |VCC - VEE| or 3.0V
- **Output Current (Q, Q)**: Continuous = 50mA
  Surge = 100mA
- **Junction-to-Ambient Thermal Resistance in Still Air**: 8-Pin µMAX = +221°C/W
  8-Pin SO = +170°C/W
- **Maximum Continuous Power Dissipation**: 8-Pin µMAX = 362mW (derate 4.5mW/°C above +70°C)
  8-Pin SO = 471mW (derate 5.9mW/°C above +70°C)
- **Junction-to-CASE Thermal Resistance**: 8-Pin µMAX = +39°C/W
  8-Pin SO = +40°C/W
- **Operating Temperature Range**: -40°C to +85°C
- **Junction Temperature**: +150°C
- **Storage Temperature Range**: -65°C to +150°C
- **ESD Protection**: Human Body Model = ±2kV
- **Soldering Temperature (10s)**: +300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

(VEE = 2.25V to 5.5V (TA = +25°C to +85°C), VCC = 2.375V to 5.5V (TA = -40°C to +25°C), outputs terminated with 50Ω ± 1% to VCC - 2.0V, unless otherwise noted. Typical values are at VCC - VEE = 3.3V, VIHD = VCC - 1.0V, VILD = VEE - 1.5V, unless otherwise noted.) (Notes 1, 2, and 3)

<table>
<thead>
<tr>
<th>PARAMETER (D, D, CLK, CLK)</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>-40°C</th>
<th>+25°C</th>
<th>+85°C</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs (D, D, CLK, CLK)</td>
<td>VIH,</td>
<td>VEE + 1.2</td>
<td>VCC</td>
<td>VEE + 1.2</td>
<td>VCC</td>
<td>VEE + 1.2</td>
</tr>
<tr>
<td></td>
<td>VILD</td>
<td>VEE</td>
<td>VEE - 0.15</td>
<td>VEE - 0.15</td>
<td>VEE</td>
<td>VEE - 0.15</td>
</tr>
<tr>
<td></td>
<td>VID</td>
<td>VCC - VEE &lt; 3.0V</td>
<td>0.15</td>
<td>VCC - VEE &lt; 3.0V</td>
<td>0.15</td>
<td>VCC - VEE &lt; 3.0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCC - VEE ≥ 3.0V</td>
<td>0.15</td>
<td>3.0</td>
<td>0.15</td>
<td>3.0</td>
</tr>
<tr>
<td>Single-Ended Input Current</td>
<td>IHI,</td>
<td>D, D, CLK, or CLK = VHIH or VILD</td>
<td>-10</td>
<td>+200</td>
<td>-10</td>
<td>+200</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OUTPUTS (Q, Q)</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>-40°C</th>
<th>+25°C</th>
<th>+85°C</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Voltage</td>
<td>VOH</td>
<td>VCC - 1.145</td>
<td>VCC - 0.895</td>
<td>VCC - 1.145</td>
<td>VCC - 0.895</td>
<td>VCC - 1.145</td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>VOL</td>
<td>VCC - 1.945</td>
<td>VCC - 1.695</td>
<td>VCC - 1.945</td>
<td>VCC - 1.695</td>
<td>VCC - 1.945</td>
</tr>
<tr>
<td>Differential Output Voltage</td>
<td>VOD</td>
<td>VOH - VOL</td>
<td>550</td>
<td>550</td>
<td>550</td>
<td>mV</td>
</tr>
</tbody>
</table>

### POWER SUPPLY

| Power-Supply Current (Note 4) | IEE | 17 | 35 | 20 | 35 | 22 | 35 | mA |
Lowest Power 3.0GHz ECL/PECL
Differential Data and Clock D Flip-Flop

AC ELECTRICAL CHARACTERISTICS

\( V_{CC} - V_{EE} = 2.25V \) to 5.5V (\( T_A = +25^\circ C \) to +85°C), \( V_{CC} - V_{EE} = 2.375V \) to 5.6V (\( T_A = -40^\circ C \) to +25°C), outputs terminated with 50Ω ±1% to \( V_{CC} - 2.0V \), \( f_{CLK} \leq 3.0GHz \), input transition time = 125ps (20% to 80%), \( V_{IH} = V_{EE} + 1.2V \) to \( V_{CC} \), \( V_{IL} = V_{EE} \) to \( V_{CC} - 0.15V \), \( V_{IH} - V_{IL} = 0.15V \) to smaller of \( |V_{CC} - V_{EE}| \) or 3V, unless otherwise noted. Typical values are at \( V_{CC} - V_{EE} = 3.3V \), \( V_{IH} = V_{CC} - 1.0V \), \( V_{IL} = V_{CC} - 1.5V \), unless otherwise noted.) (Notes 1, 5)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>-40°C</th>
<th>+25°C</th>
<th>+85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>t_{PHL}</td>
<td>Figure 2</td>
<td>370</td>
<td>328</td>
<td>405</td>
</tr>
<tr>
<td></td>
<td>t_{PLH}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Clock Frequency</td>
<td>f_{CLK}</td>
<td>VOD ≥ 300mV</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Setup Time</td>
<td>t_S</td>
<td>Figure 2</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Hold Time</td>
<td>t_H</td>
<td>Figure 2</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Added Random Jitter (Note 6)</td>
<td>t_{RJ}</td>
<td></td>
<td>0.2</td>
<td>0.8</td>
<td>0.2</td>
</tr>
<tr>
<td>Differential Output Rise/Fall Time</td>
<td>t_{RF}</td>
<td>20% to 80%, Figure 2</td>
<td>70</td>
<td>120</td>
<td>170</td>
</tr>
</tbody>
</table>

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterization over the full operating temperature range.
Note 4: All pins floating except \( V_{CC} \) and \( V_{EE} \).
Note 5: Guaranteed by design and characterization, and are not production tested. Limits are set to ±6 sigma.
Note 6: Device jitter added to the input clock.
Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

Typical Operating Characteristics

($V_{CC} - V_{EE} = 3.3V$, outputs loaded with 50Ω ±1% to $V_{CC} - 2V$, $V_{IH} = V_{CC} - 1V$, $V_{IL} = V_{CC} - 1.5V$, $f_{CLK} = 3GHz$, $I_{D} = f_{CLK}/2$ input transition time = 125ps (20% to 80%), unless otherwise noted.)
Detailed Description

The MAX9381 D flip-flop transfers the logic level at the D input to the Q output on a rising edge transition of the clock, provided the minimum setup and hold times are met. By interchanging the CLK and \( \overline{CLK} \) inputs, the flip-flop functions as a falling-edge triggered flip-flop.

The input signals (D, \( \overline{D} \), and CLK, \( \overline{CLK} \)) are differential and have a maximum differential input voltage of 3.0V or VCC - VEE, whichever is less. To ensure that the outputs remain stable when the inputs are left open, each of the inputs is driven low by a 75k\( \Omega \) bias resistor connected to VEE. If the D and \( \overline{D} \) inputs are left open or at VEE, the output is guaranteed to be a differential low on the next low-to-high transition of the clock. If the CLK and \( \overline{CLK} \) inputs are left open or at VEE, the outputs remain unchanged (Table 1). Terminate the outputs (Q, \( \overline{Q} \)) through 50\( \Omega \) to VCC - 2V or an equivalent Thevenin termination (see the Output Termination section).

ECL/PECL Operation

Output levels are referenced to VCC and are considered PECL or ECL, depending on the level of the VCC supply. With VCC connected to a positive supply and VEE connected to GND, the outputs are PECL. The outputs are ECL when VCC is connected to GND and VEE is connected to a negative supply.

Applications Information

T Flip-Flop

The MAX9381 can be configured as a T flip-flop by connecting Q to D and \( \overline{Q} \) to D. This configuration provides an output at half the frequency of the clock. The maximum operating frequency is determined by the sum of the setup time, the propagation delay of the

Table 1. Truth Table*

<table>
<thead>
<tr>
<th>D, ( \overline{D} )</th>
<th>CLK, ( \overline{CLK} )</th>
<th>Q, ( \overline{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
<td>H</td>
</tr>
<tr>
<td>Open or VEE</td>
<td>↑</td>
<td>L</td>
</tr>
<tr>
<td>X</td>
<td>Open or VEE</td>
<td>No change</td>
</tr>
</tbody>
</table>

*Where logic states are differential, ↑ is a low-to-high transition and X signifies a don’t care state.

Figure 1. Input and Output Voltage Definitions

Figure 1. Input and Output Voltage Definitions
Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

Device and any added delay by circuit board traces. The minimum supply voltage is 2.375V and is determined by input and output voltage range.

**Output Termination**

Terminate the outputs through 50Ω to \( \text{VCC} - 2V \) or use equivalent Thevenin terminations. Terminate each \( Q \) and \( \bar{Q} \) outputs with identical termination on each for the lowest output distortion. When a single-ended signal is taken from the differential output, terminate both \( Q \) and \( \bar{Q} \).

Ensure that output currents do not exceed the current limits as specified in the Absolute Maximum Ratings table. Under all operating conditions, the device’s total thermal limits should be observed.

**Power-Supply Bypassing**

Bypass \( \text{VCC} \) to \( \text{VEE} \) with high-frequency surface-mount ceramic 0.1μF and 0.01μF capacitors. Place the capacitors as close to the device as possible with the 0.01μF capacitor closest to the device pins.

Use multiple vias when connecting the bypass capacitors to ground. This reduces trace inductance, which lowers power-supply bounce when drawing high transient currents.

**Circuit Board Traces**

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners, or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

**Chip Information**

TRANSISTOR COUNT: 375
PROCESS: Bipolar

![Figure 2. CLK-to-Q Propagation Delay and Transition Timing Diagram](image-url)
Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

NOTES:
1. FILE DOES NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006”).
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MS-022 AA.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

© 2002 Maxim Integrated Products Printed USA Maxim is a registered trademark of Maxim Integrated Products.